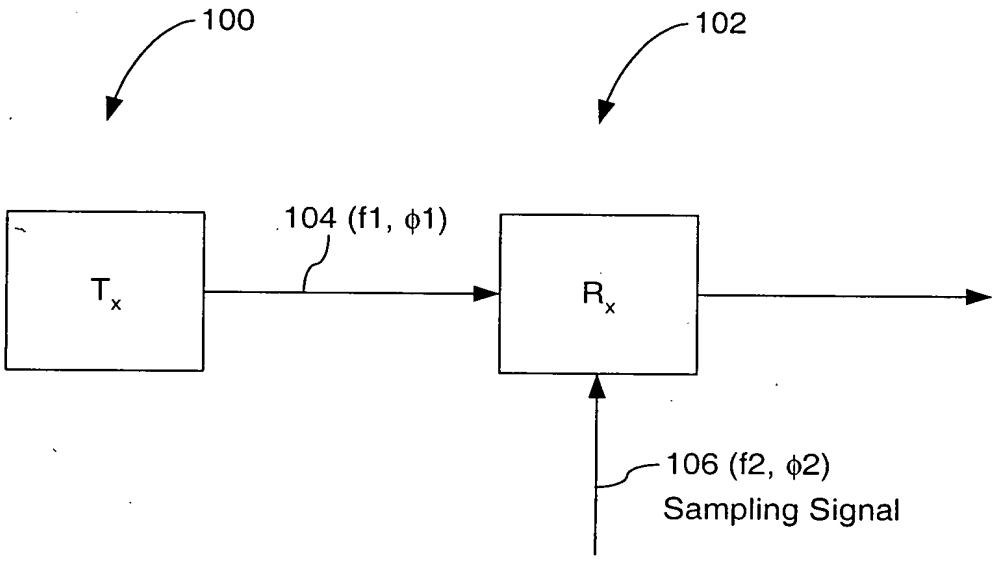


FIG. 1

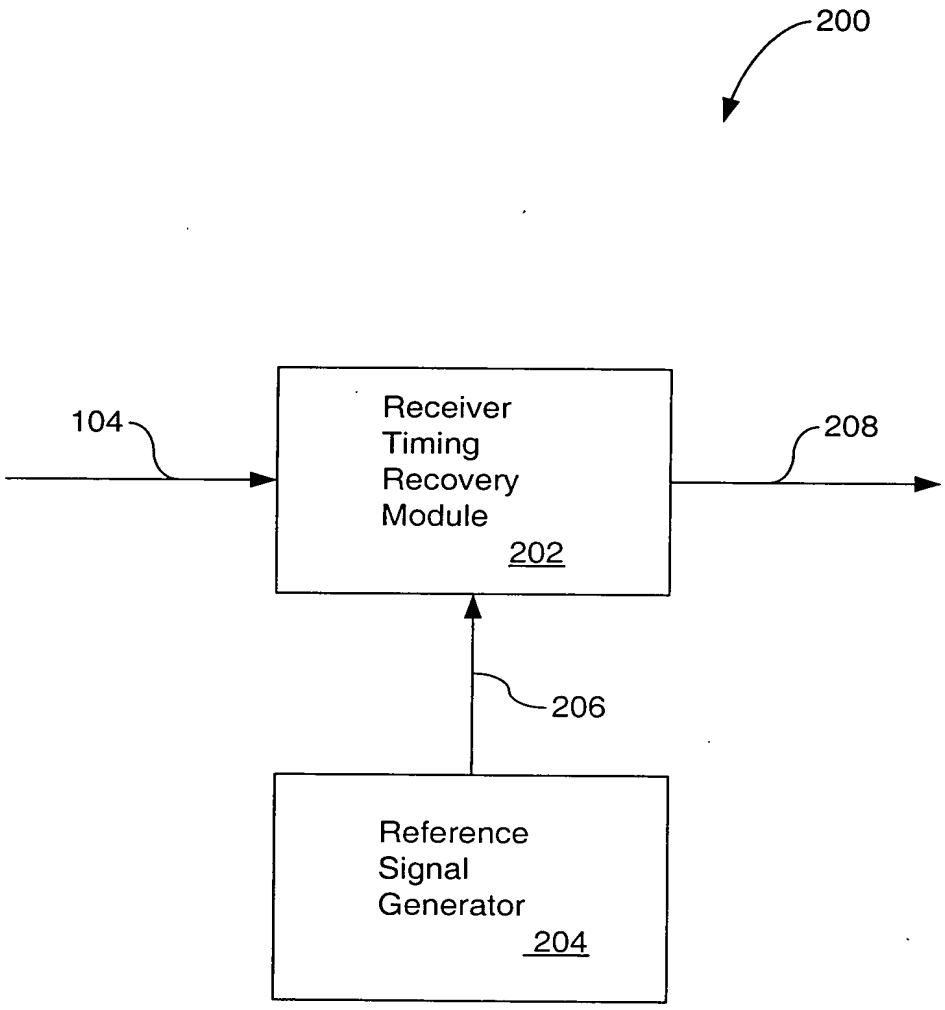

200
104
Receiver
Timing
Recovery
Module
202
208
206
Reference
Signal
Generator
204

FIG. 2

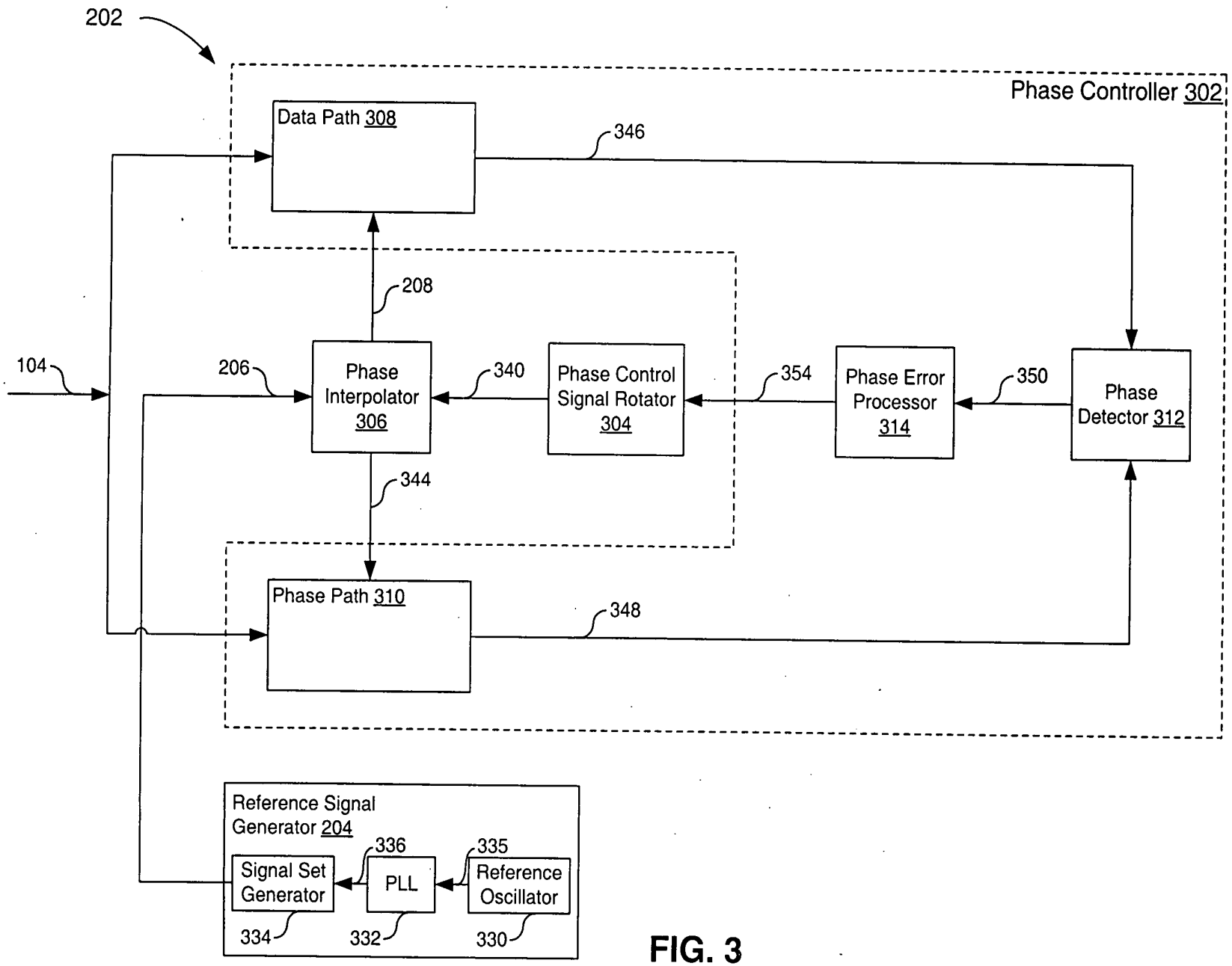

202
Phase Controller 302
Data Path 308
346
208
104
206
Phase Interpolator 306
340
Phase Control Signal Rotator 304
354
Phase Error Processor 314
350
Phase Detector 312
344
Phase Path 310
348
Reference Signal Generator 204
336
335
Signal Set Generator
PLL
Reference Oscillator
334
332
330

FIG. 3

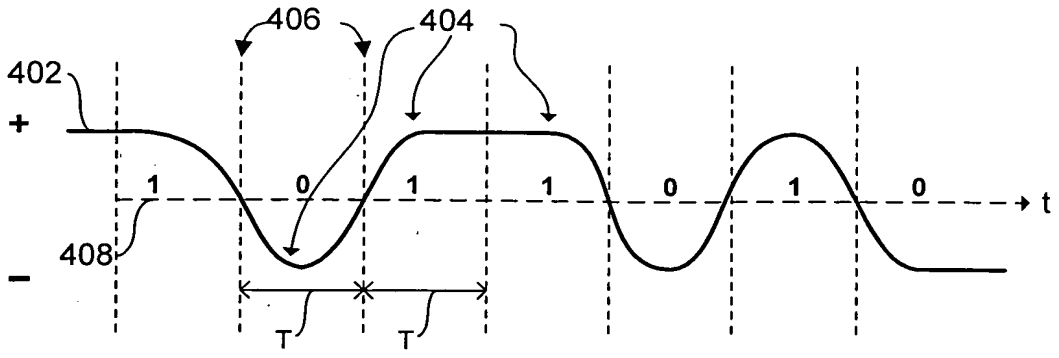


FIG. 4A

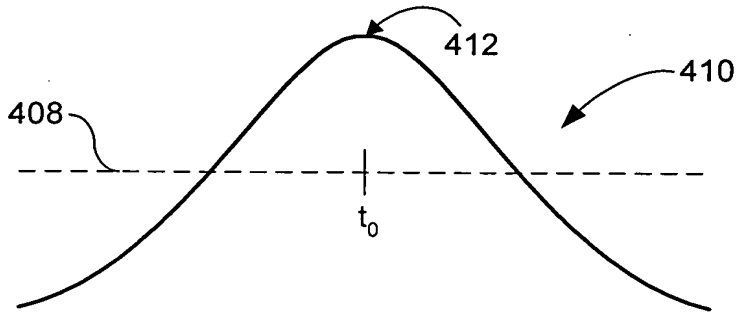


FIG. 4B

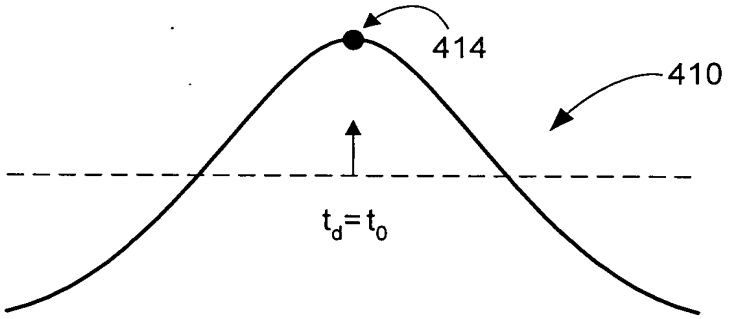


FIG. 4C

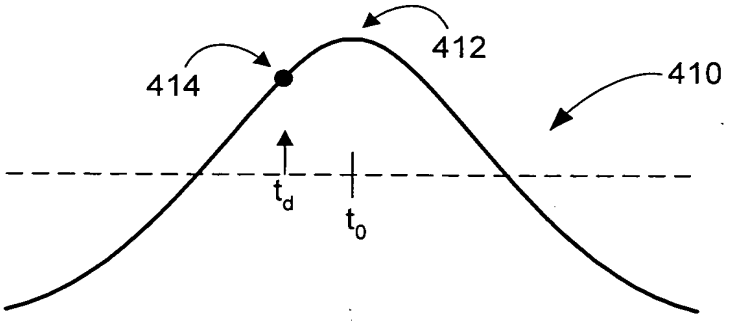


FIG. 4D

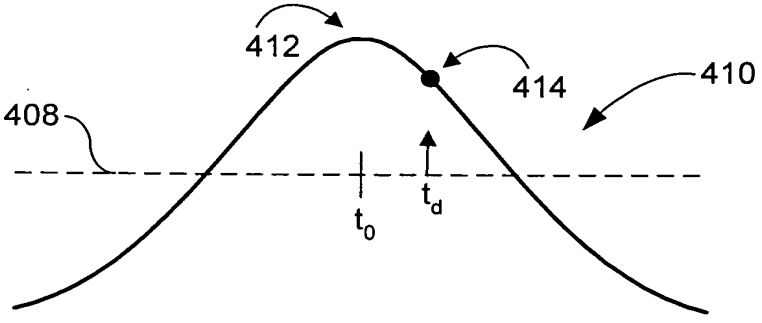


FIG. 4E

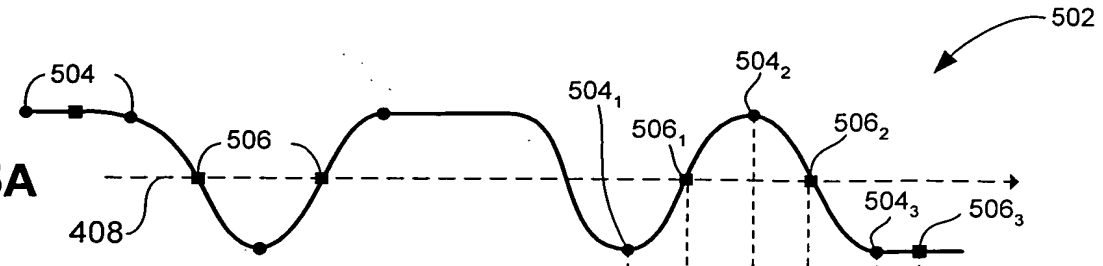


FIG. 5A

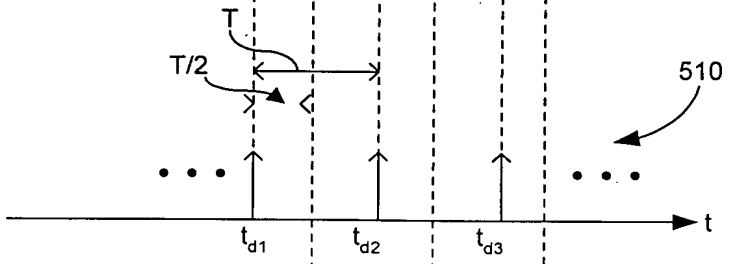


FIG. 5B

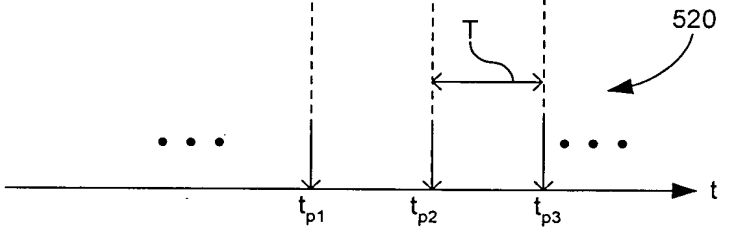


FIG. 5C

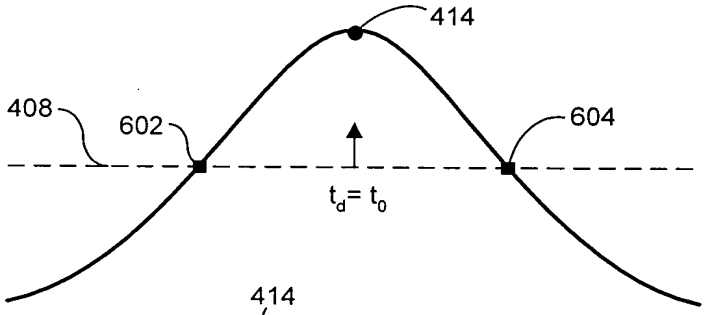


FIG. 6A

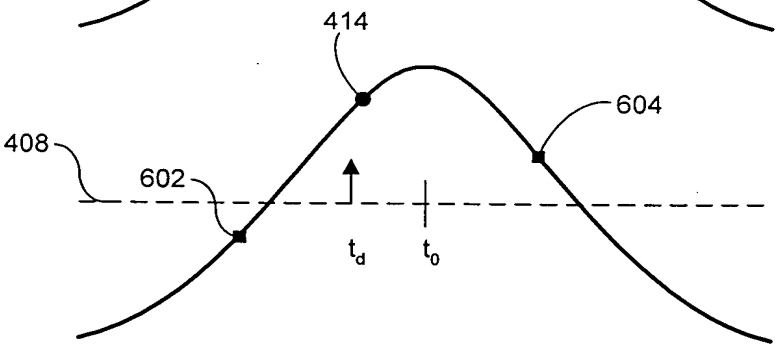


FIG. 6B

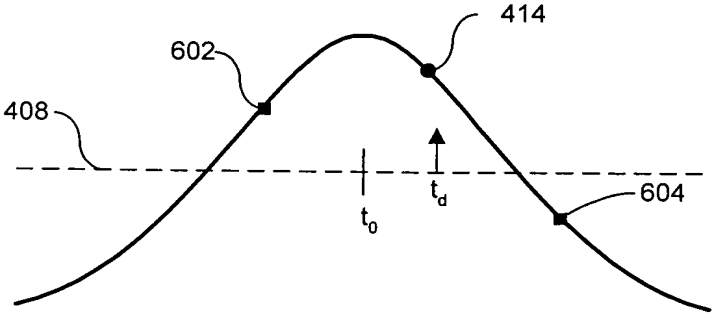


FIG. 6C

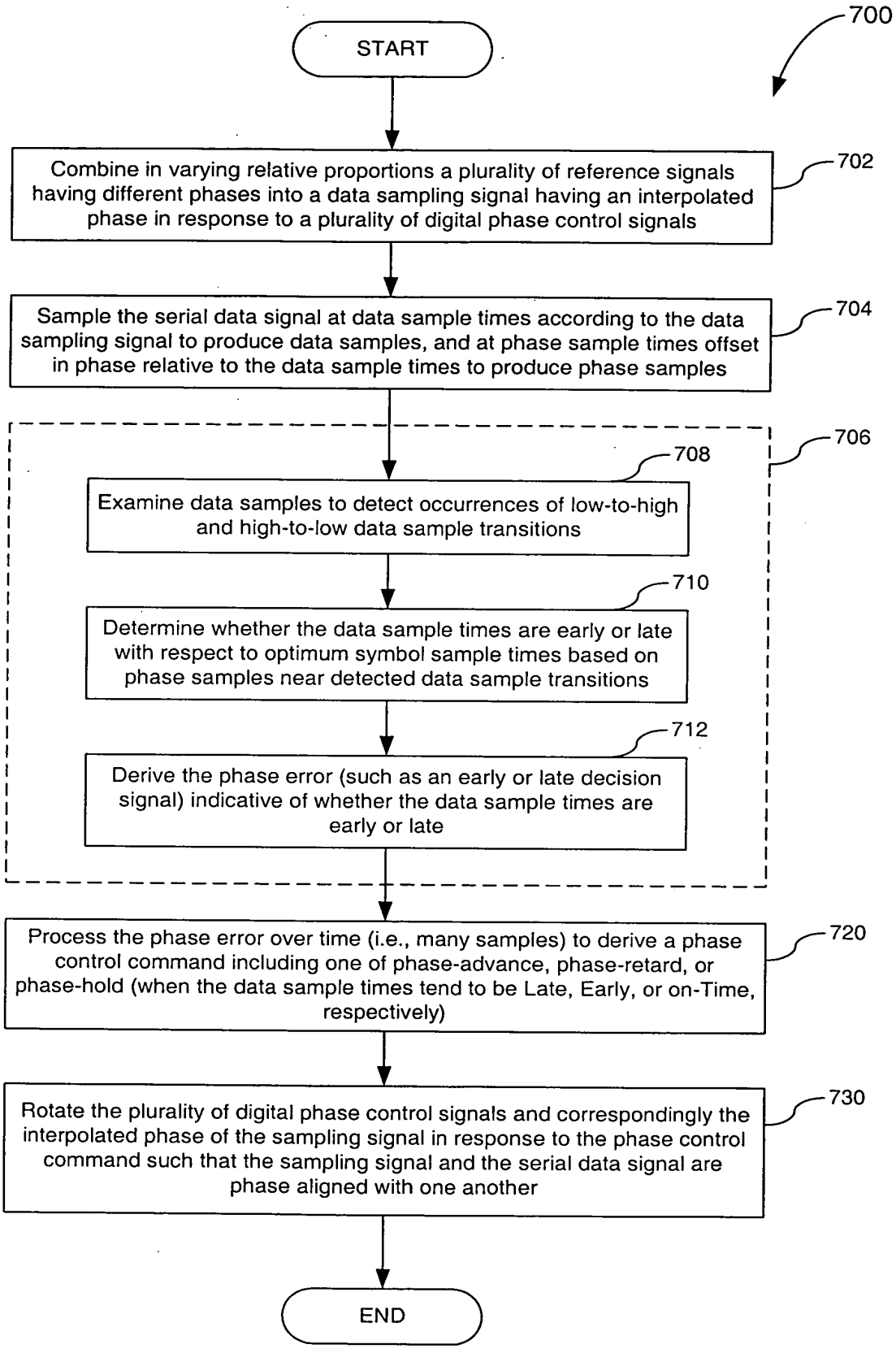

700
START
Combine in varying relative proportions a plurality of reference signals having different phases into a data sampling signal having an interpolated phase in response to a plurality of digital phase control signals
702
Sample the serial data signal at data sample times according to the data sampling signal to produce data samples, and at phase sample times offset in phase relative to the data sample times to produce phase samples
704
706
708
Examine data samples to detect occurrences of low-to-high and high-to-low data sample transitions
710
Determine whether the data sample times are early or late with respect to optimum symbol sample times based on phase samples near detected data sample transitions
712
Derive the phase error (such as an early or late decision signal) indicative of whether the data sample times are early or late
Process the phase error over time (i.e., many samples) to derive a phase control command including one of phase-advance, phase-retard, or phase-hold (when the data sample times tend to be Late, Early, or on-Time, respectively)
720
Rotate the plurality of digital phase control signals and correspondingly the interpolated phase of the sampling signal in response to the phase control command such that the sampling signal and the serial data signal are phase aligned with one another
730
END

FIG. 7

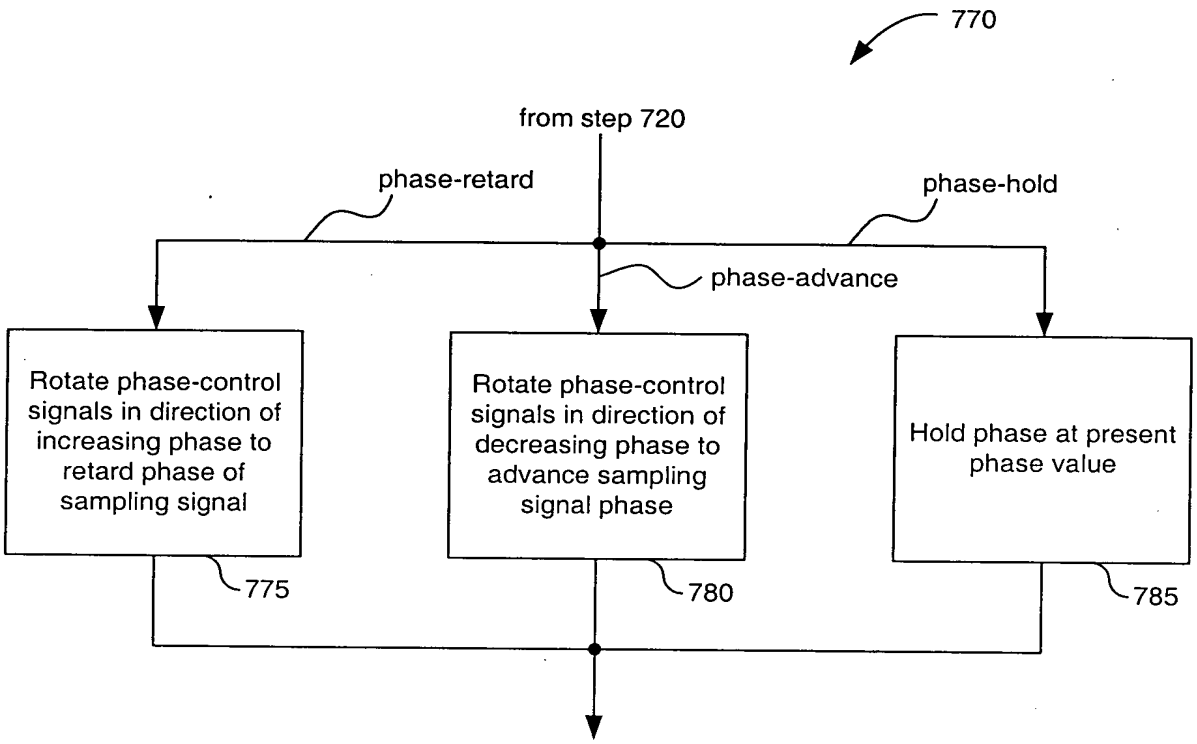

770
from step 720
phase-retard
phase-hold
phase-advance
Rotate phase-control signals in direction of increasing phase to retard phase of sampling signal
Rotate phase-control signals in direction of decreasing phase to advance sampling signal phase
Hold phase at present phase value
775
780
785

FIG. 7A

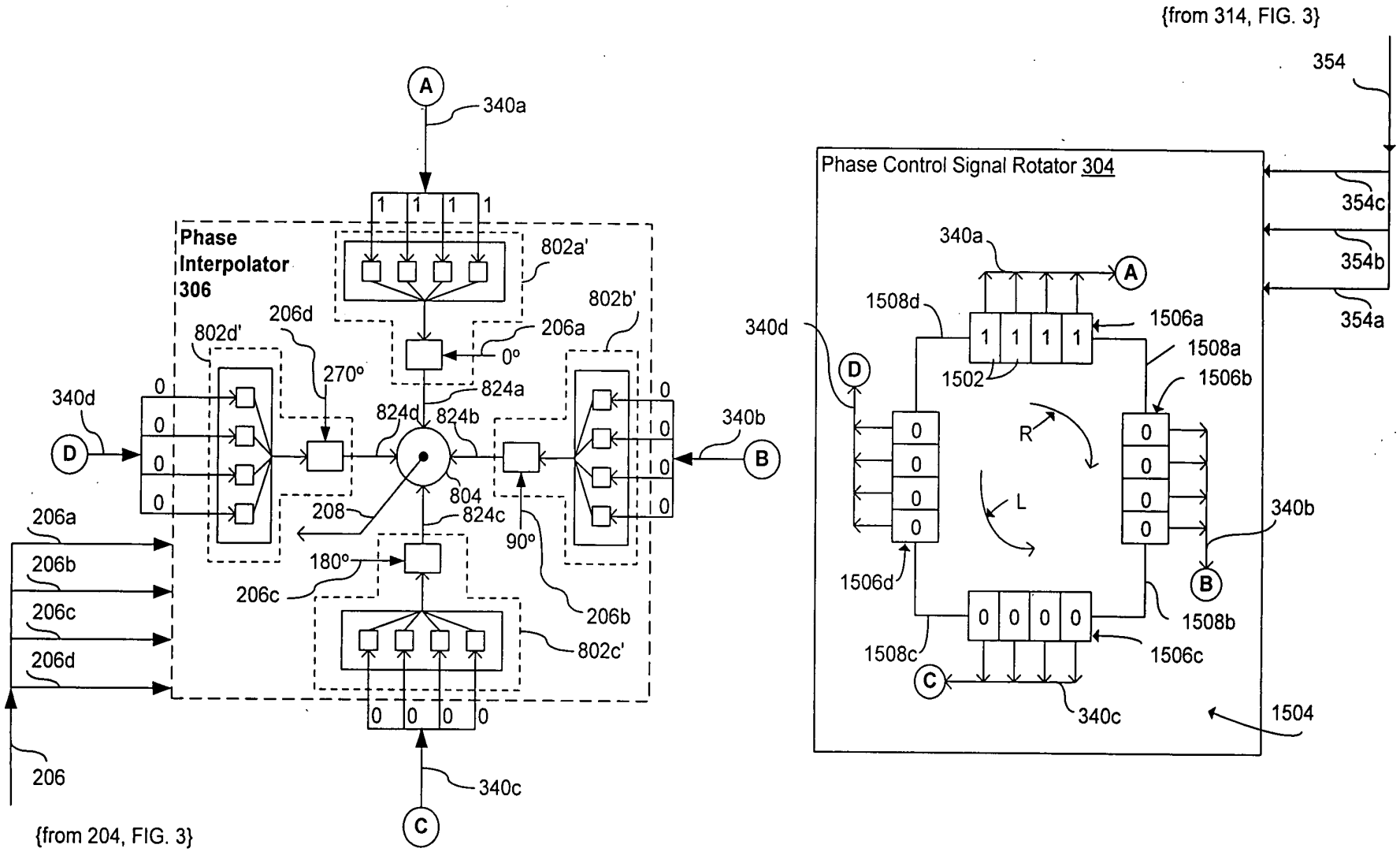

{from 314, FIG. 3}
354
Phase Control Signal Rotator 304
354c
354b
354a
340a
A
1508d
1506a
1508a
1506b
340d
D
1502
R
L
340b
B
1506d
1508b
1508c
1506c
C
340c
1504
Phase Interpolator 306
802a'
802b'
802d'
206d
206a
0°
270°
824a
824d
824b
340d
340b
804
208
824c
90°
206a
206b
206c
206d
180°
206c
206b
802c'
206
340c
{from 204, FIG. 3}

FIG. 15

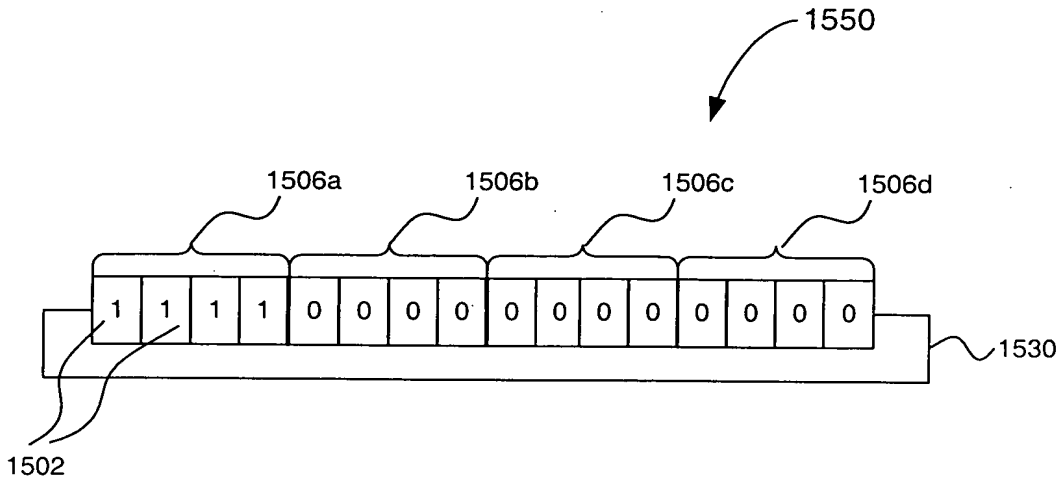


FIG. 15A

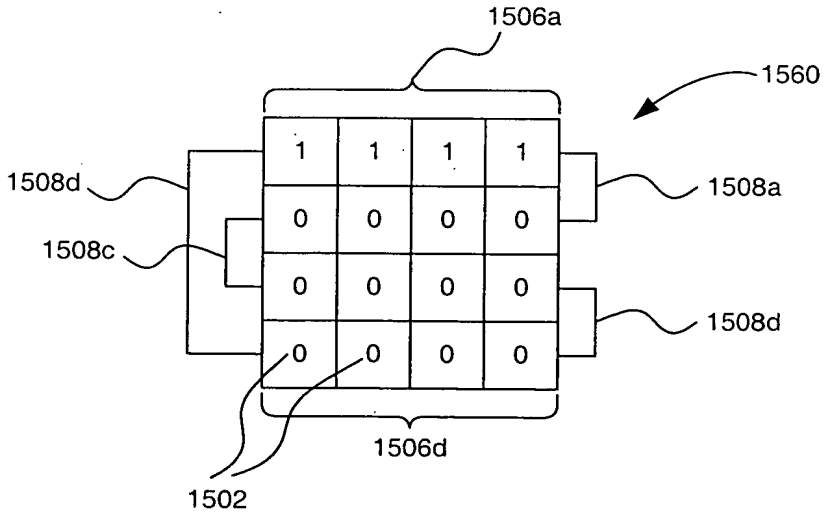


FIG. 15B

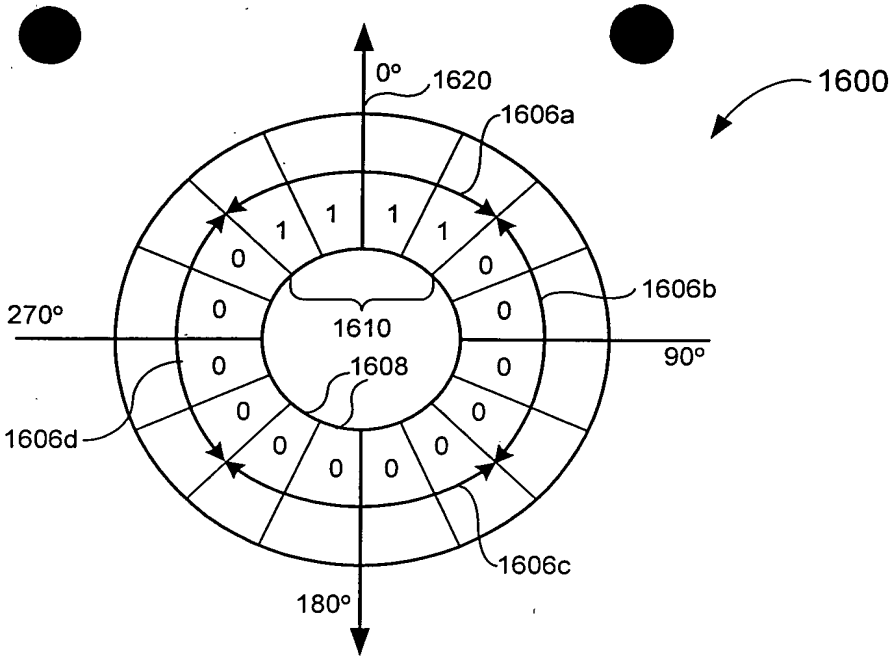


FIG. 16A

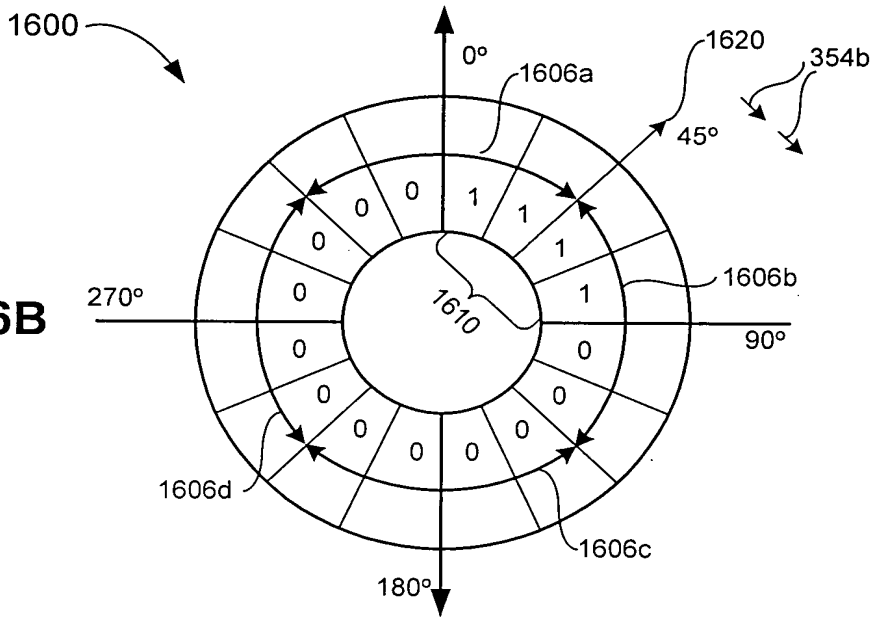


FIG. 16B

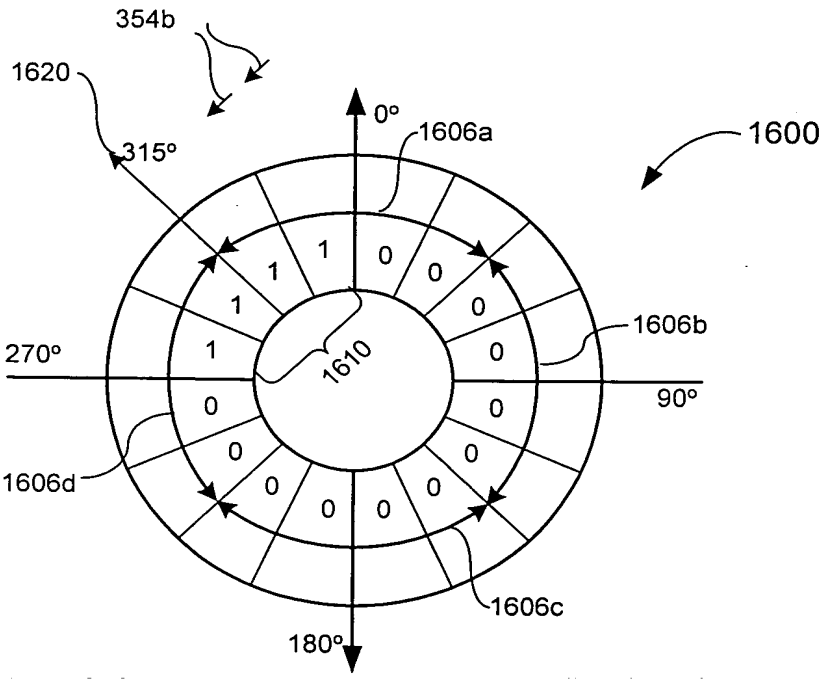


FIG. 16C

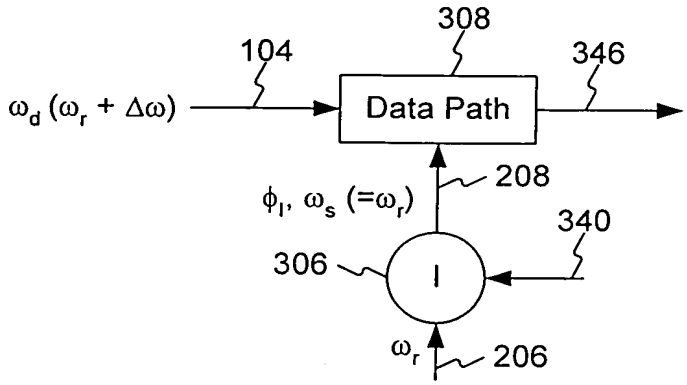

308
104
346
ω_d (ω_r + $\Delta\omega$)
Data Path
208
ϕ_I, ω_s (=ω_r)
340
306
I
ω_r
206

FIG. 17

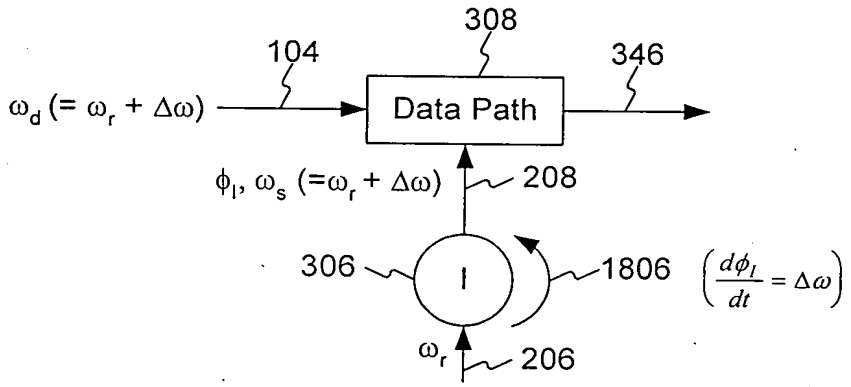

308
104
346
ω_d (= ω_r + $\Delta\omega$)
Data Path
ϕ_I, ω_s (=ω_r + $\Delta\omega$)
208
306
I
1806
$\left(\frac{d\phi_I}{dt} = \Delta\omega\right)$
ω_r
206

FIG. 18

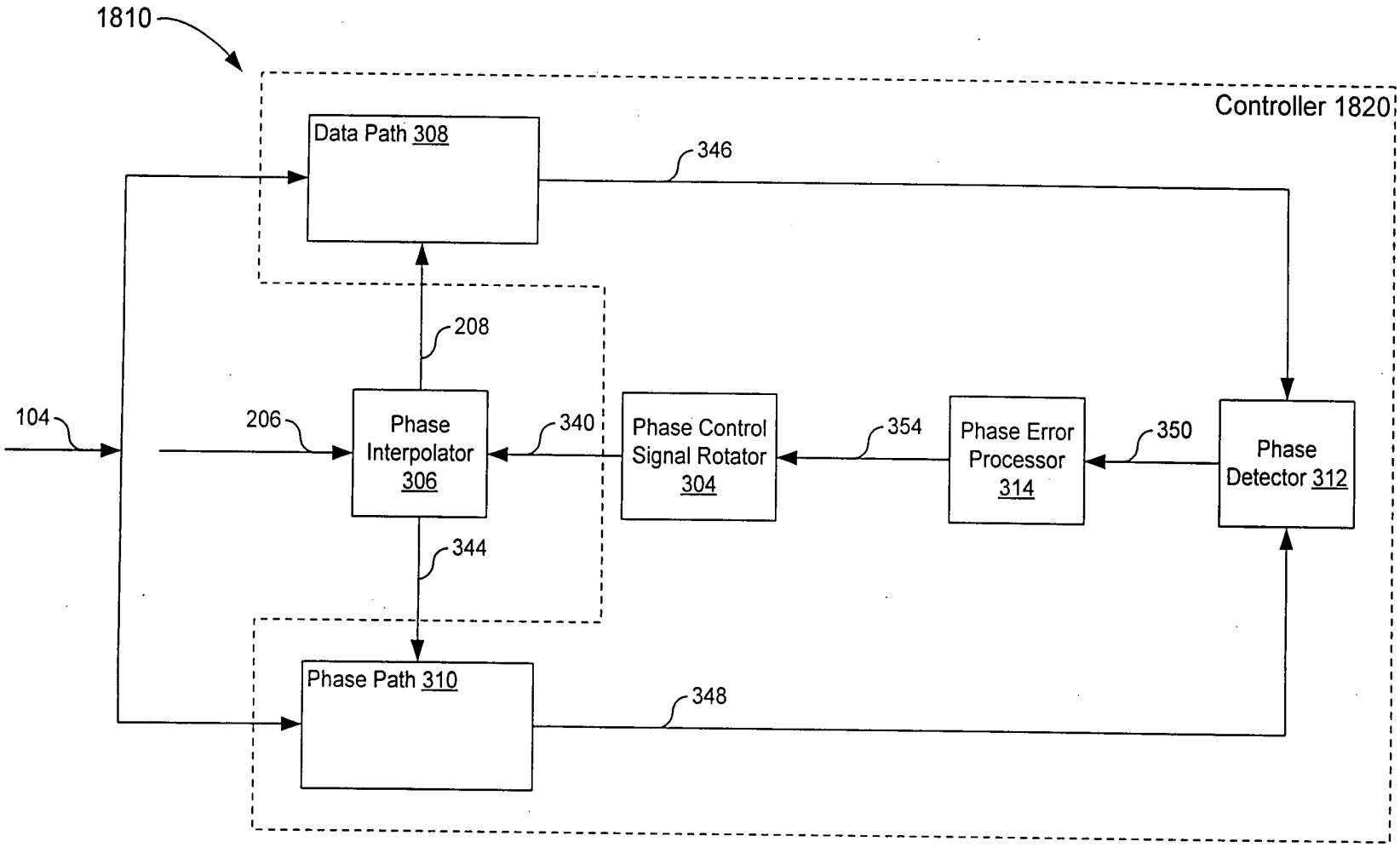

1810
Controller 1820
Data Path 308
346
208
104
206
Phase Interpolator 306
340
Phase Control Signal Rotator 304
354
Phase Error Processor 314
350
Phase Detector 312
344
Phase Path 310
348

FIG. 18A

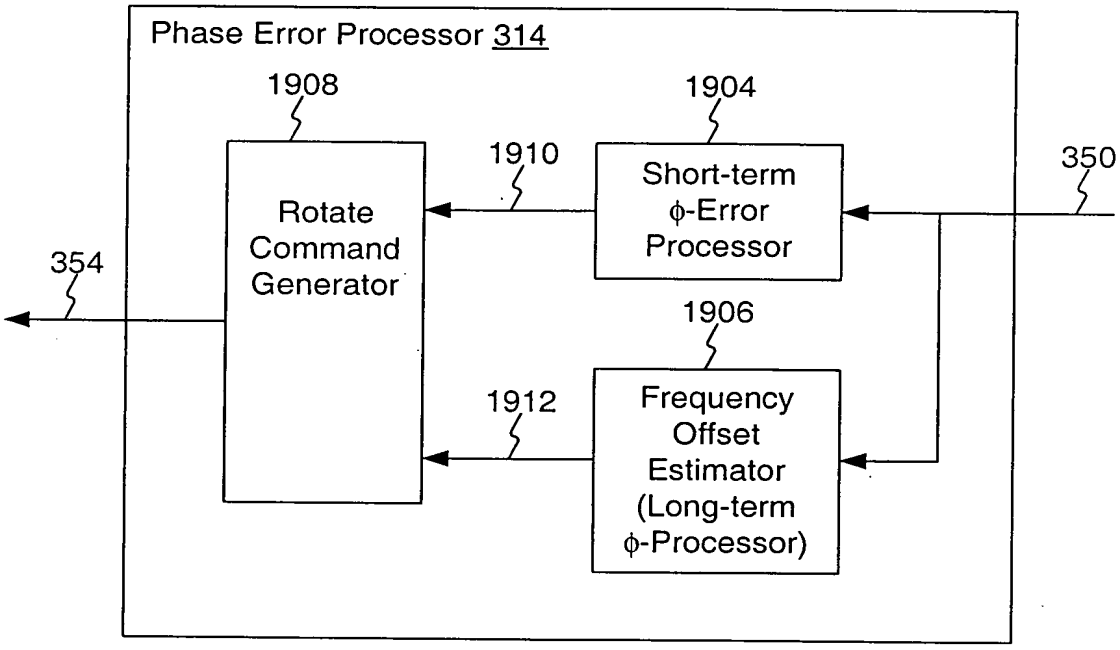

Phase Error Processor 314
1908
1904
1910
350
Rotate Command Generator
Short-term ϕ-Error Processor
354
1906
1912
Frequency Offset Estimator (Long-term ϕ-Processor)

FIG. 19

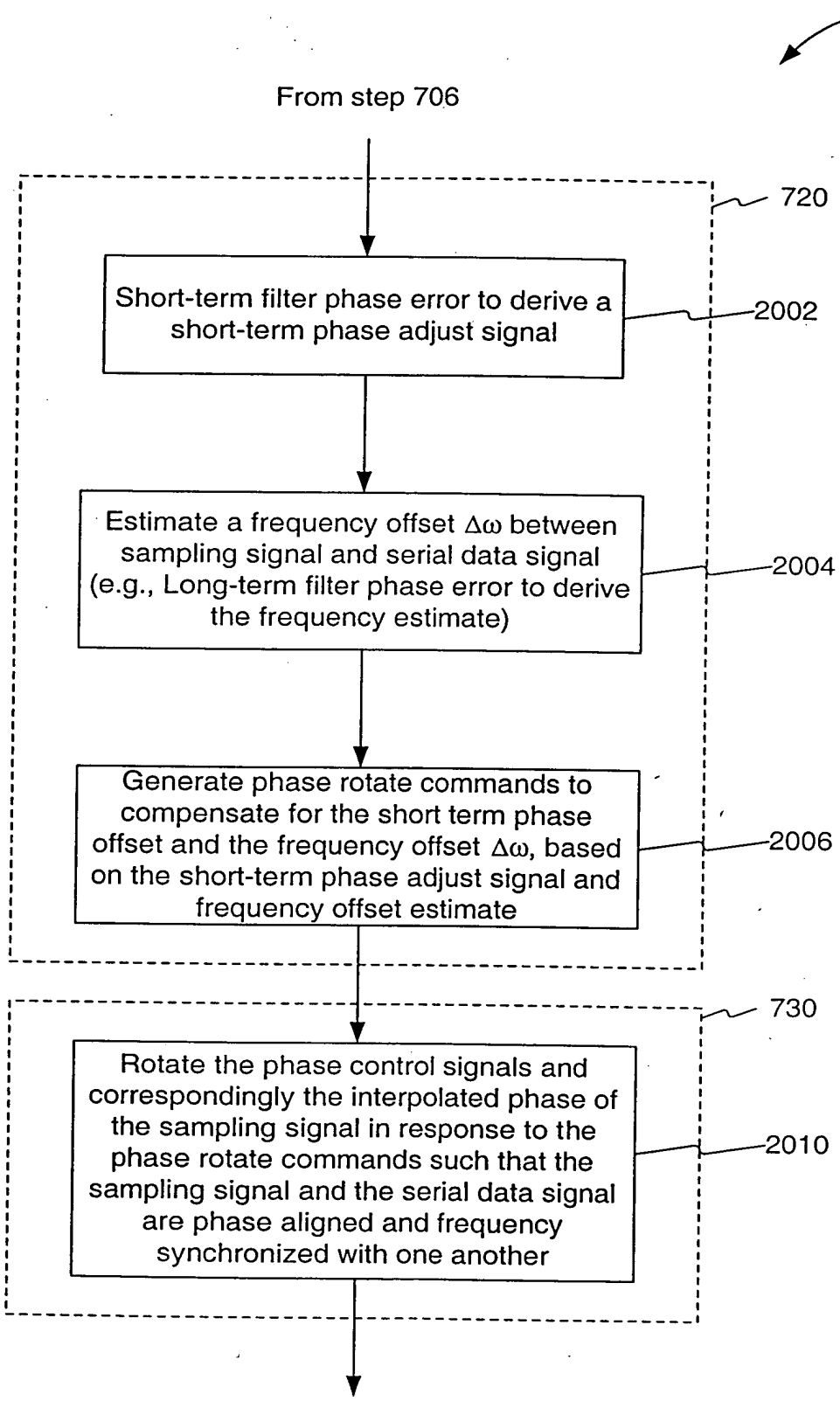

2000
From step 706
720
Short-term filter phase error to derive a short-term phase adjust signal
2002
Estimate a frequency offset Δω between sampling signal and serial data signal (e.g., Long-term filter phase error to derive the frequency estimate)
2004
Generate phase rotate commands to compensate for the short term phase offset and the frequency offset Δω, based on the short-term phase adjust signal and frequency offset estimate
2006
730
Rotate the phase control signals and correspondingly the interpolated phase of the sampling signal in response to the phase rotate commands such that the sampling signal and the serial data signal are phase aligned and frequency synchronized with one another
2010

FIG. 20

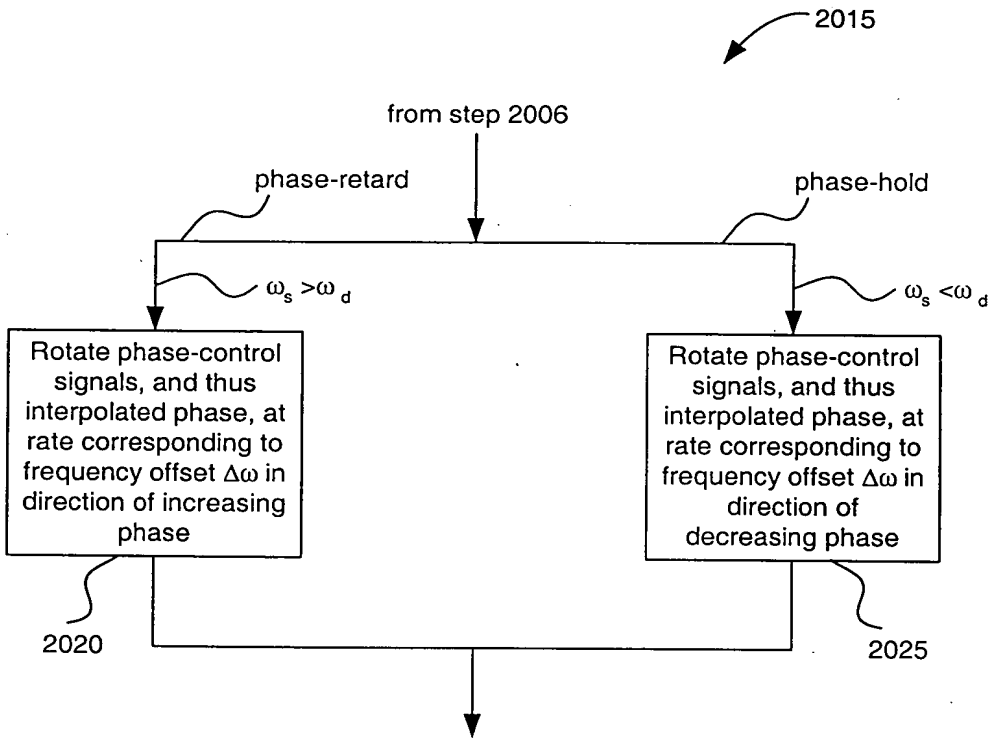

2015
from step 2006
phase-retard
phase-hold
$\omega_s > \omega_d$
$\omega_s < \omega_d$
Rotate phase-control signals, and thus interpolated phase, at rate corresponding to frequency offset $\Delta\omega$ in direction of increasing phase
Rotate phase-control signals, and thus interpolated phase, at rate corresponding to frequency offset $\Delta\omega$ in direction of decreasing phase
2020
2025

FIG. 20A

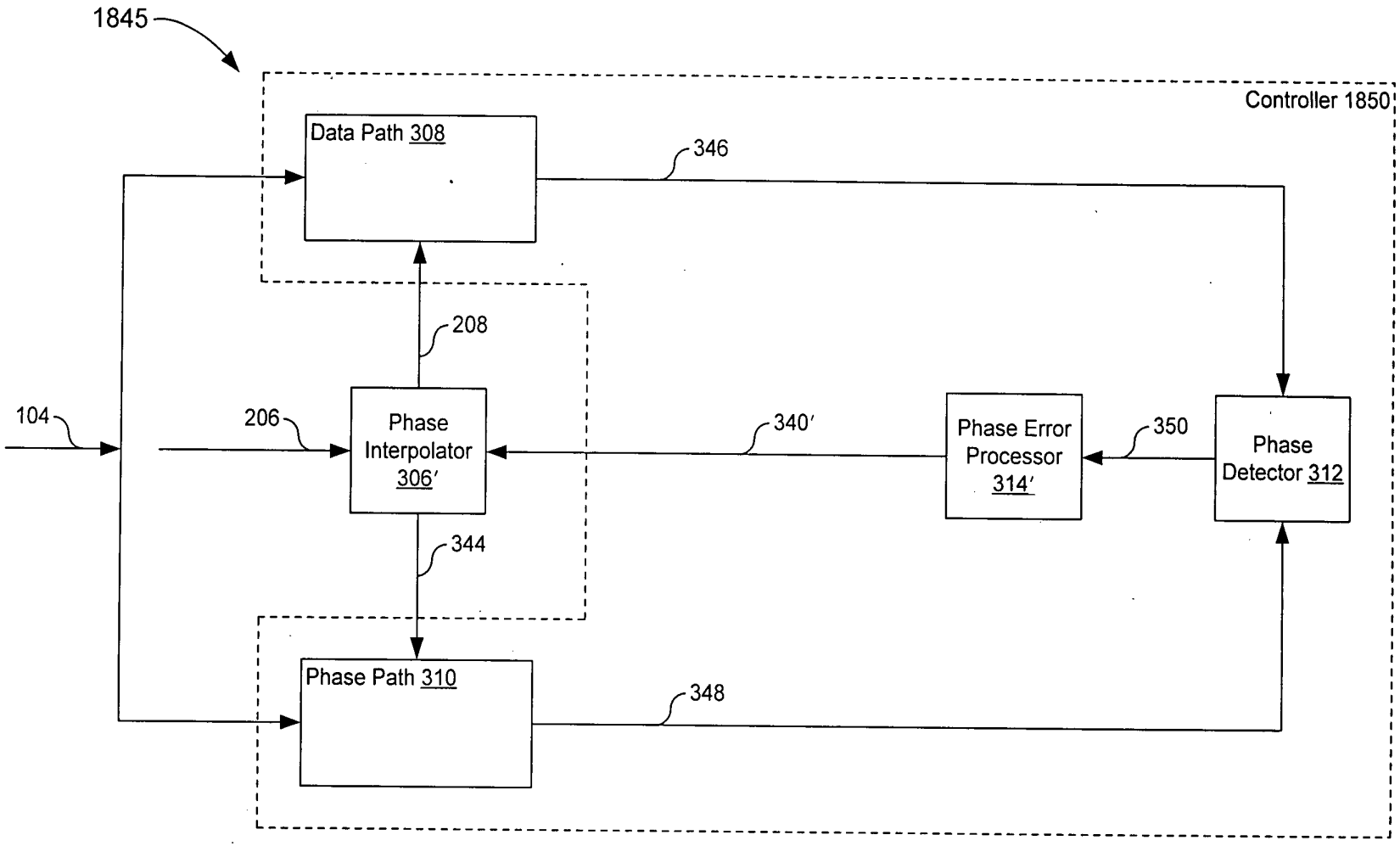

1845
Controller 1850
Data Path 308
346
208
104
206
Phase Interpolator 306'
340'
Phase Error Processor 314'
350
Phase Detector 312
344
Phase Path 310
348

FIG. 20B

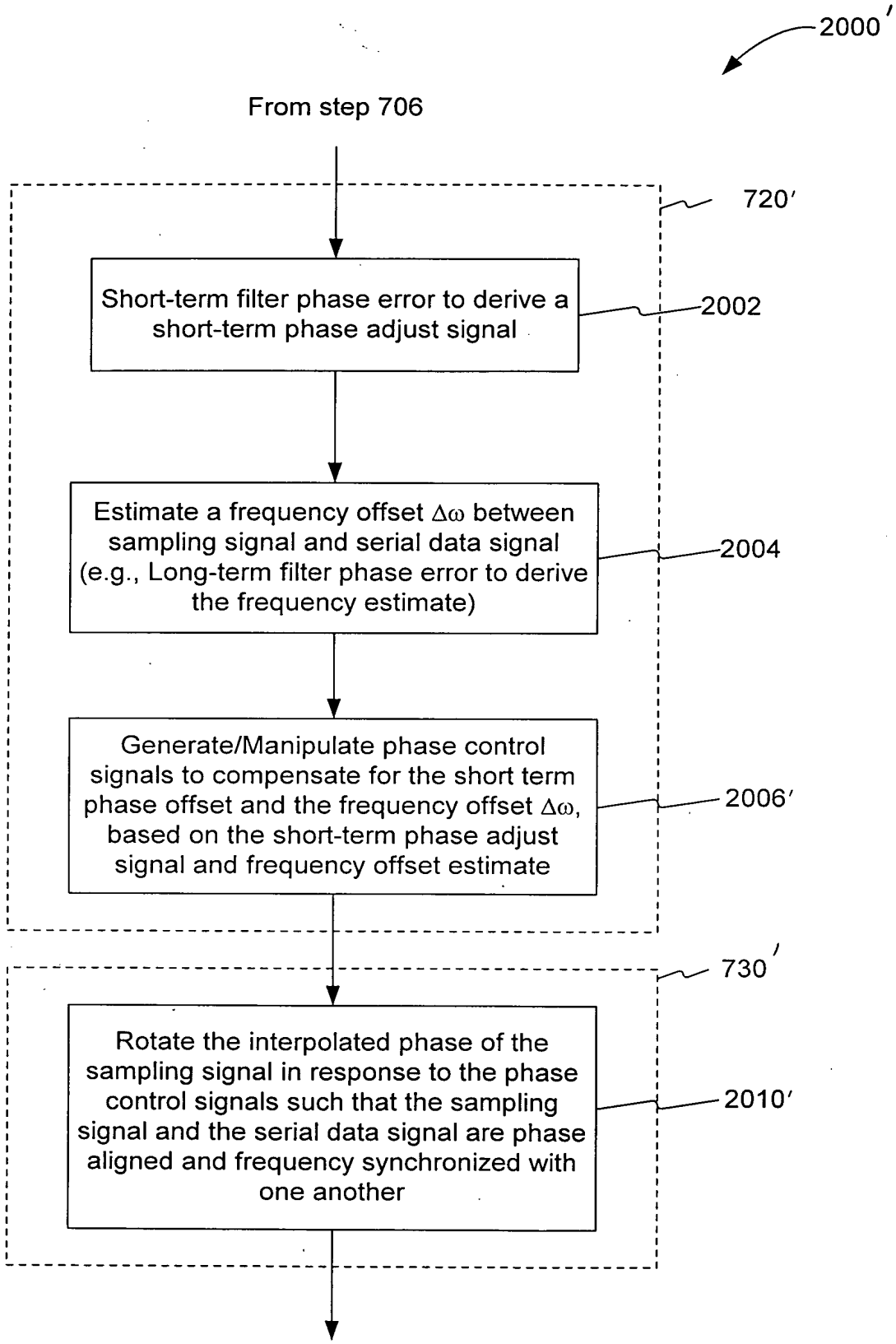

2000'
From step 706
720'
Short-term filter phase error to derive a short-term phase adjust signal
2002
Estimate a frequency offset Δω between sampling signal and serial data signal (e.g., Long-term filter phase error to derive the frequency estimate)
2004
Generate/Manipulate phase control signals to compensate for the short term phase offset and the frequency offset Δω, based on the short-term phase adjust signal and frequency offset estimate
2006'
730'
Rotate the interpolated phase of the sampling signal in response to the phase control signals such that the sampling signal and the serial data signal are phase aligned and frequency synchronized with one another
2010'

FIG. 20C

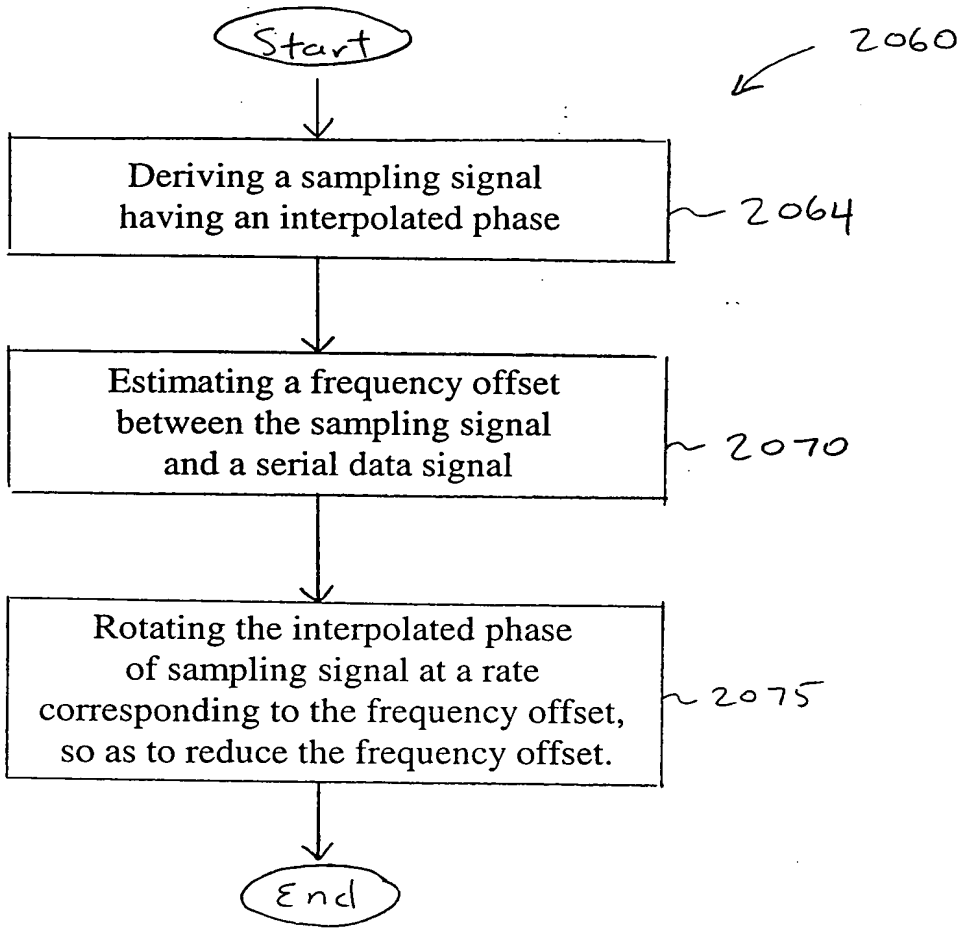
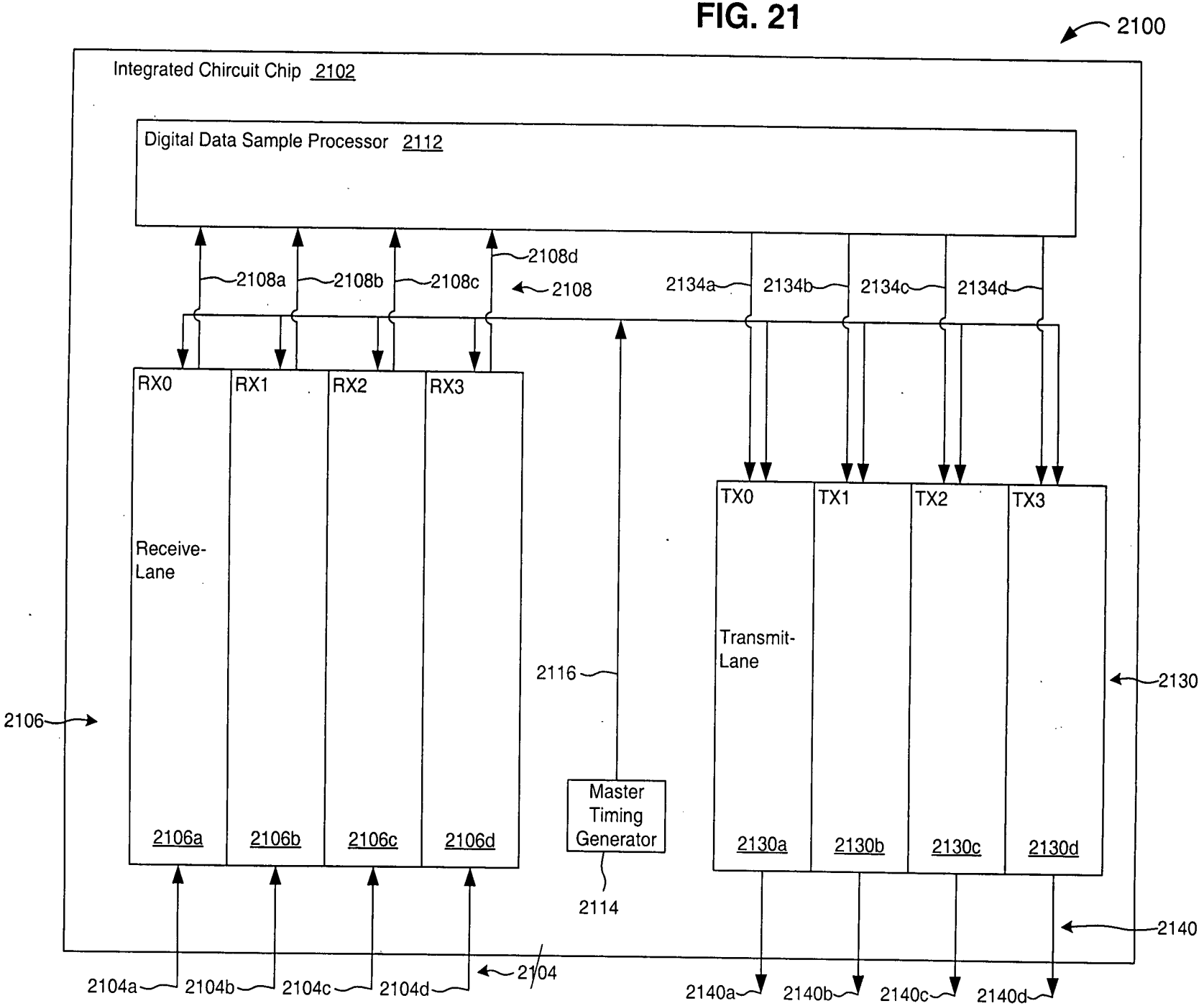

Start
2060
Deriving a sampling signal having an interpolated phase
2064
Estimating a frequency offset between the sampling signal and a serial data signal
2070
Rotating the interpolated phase of sampling signal at a rate corresponding to the frequency offset, so as to reduce the frequency offset.
2075
End

FIG. 20D

FIG. 21


2100
Integrated Chircuit Chip 2102
Digital Data Sample Processor 2112
2108a
2108b
2108c
2108d
2108
2134a
2134b
2134c
2134d
RX0
RX1
RX2
RX3
Receive-Lane
2106a
2106b
2106c
2106d
2106
2116
Master Timing Generator
2114
TX0
TX1
TX2
TX3
Transmit-Lane
2130a
2130b
2130c
2130d
2130
2140
2104a
2104b
2104c
2104d
2104
2140a
2140b
2140c
2140d

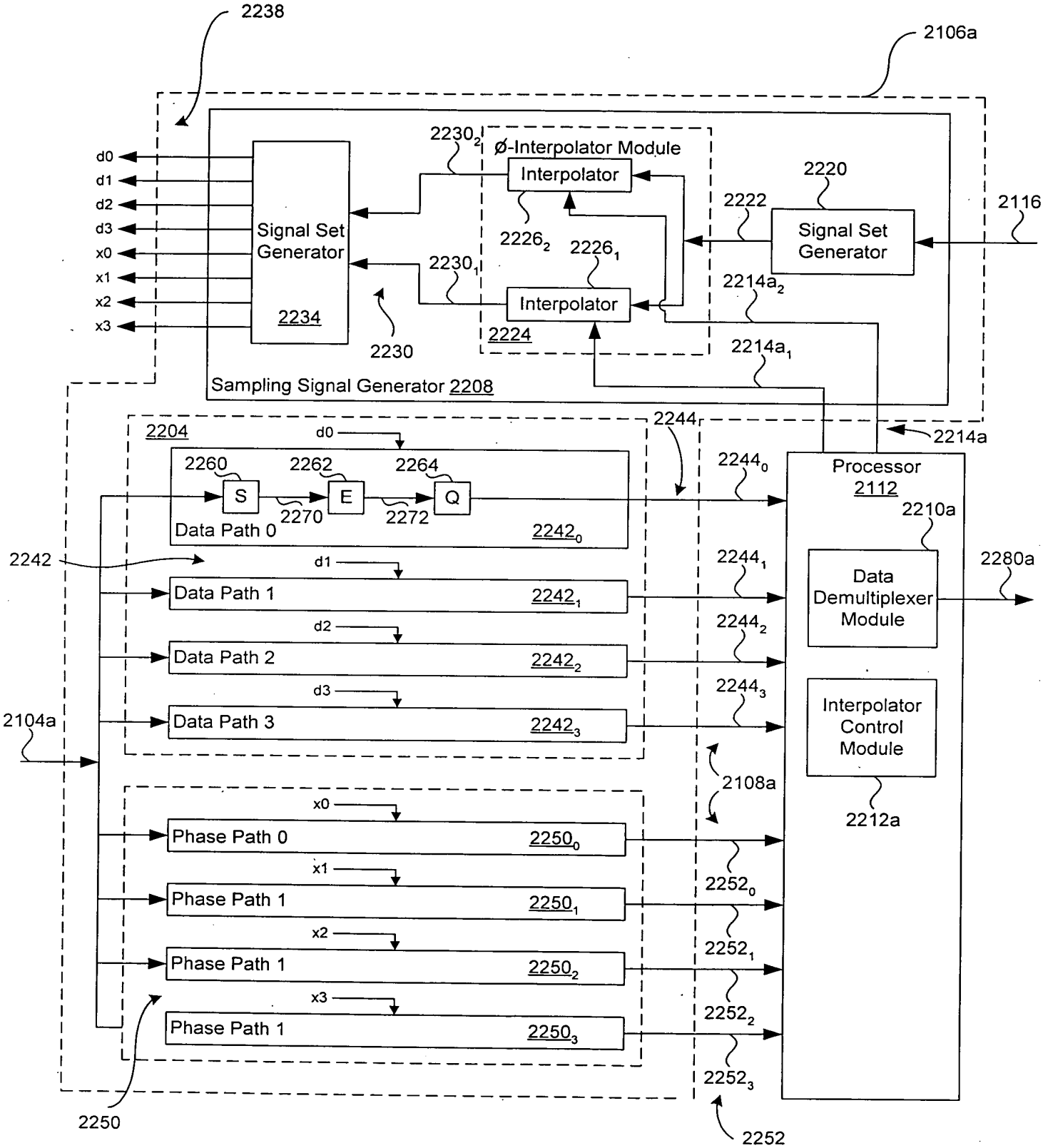

2238
2106a
d0
d1
d2
d3
x0
x1
x2
x3
Signal Set Generator
2234
2230
2230₂
Ø-Interpolator Module
Interpolator
2226₂
2226₁
2230₁
Interpolator
2224
2220
2222
Signal Set Generator
2116
2214a₂
2214a₁
Sampling Signal Generator 2208
2204
d0
2260
2262
2264
S
E
Q
2270
2272
Data Path 0
2242₀
2242
d1
Data Path 1
2242₁
d2
Data Path 2
2242₂
d3
Data Path 3
2242₃
2104a
2244
2244₀
2244₁
2244₂
2244₃
2214a
Processor 2112
2210a
Data Demultiplexer Module
2280a
Interpolator Control Module
2212a
2108a
x0
Phase Path 0
2250₀
x1
Phase Path 1
2250₁
x2
Phase Path 1
2250₂
x3
Phase Path 1
2250₃
2250
2252₀
2252₁
2252₂
2252₃
2252

FIG. 22

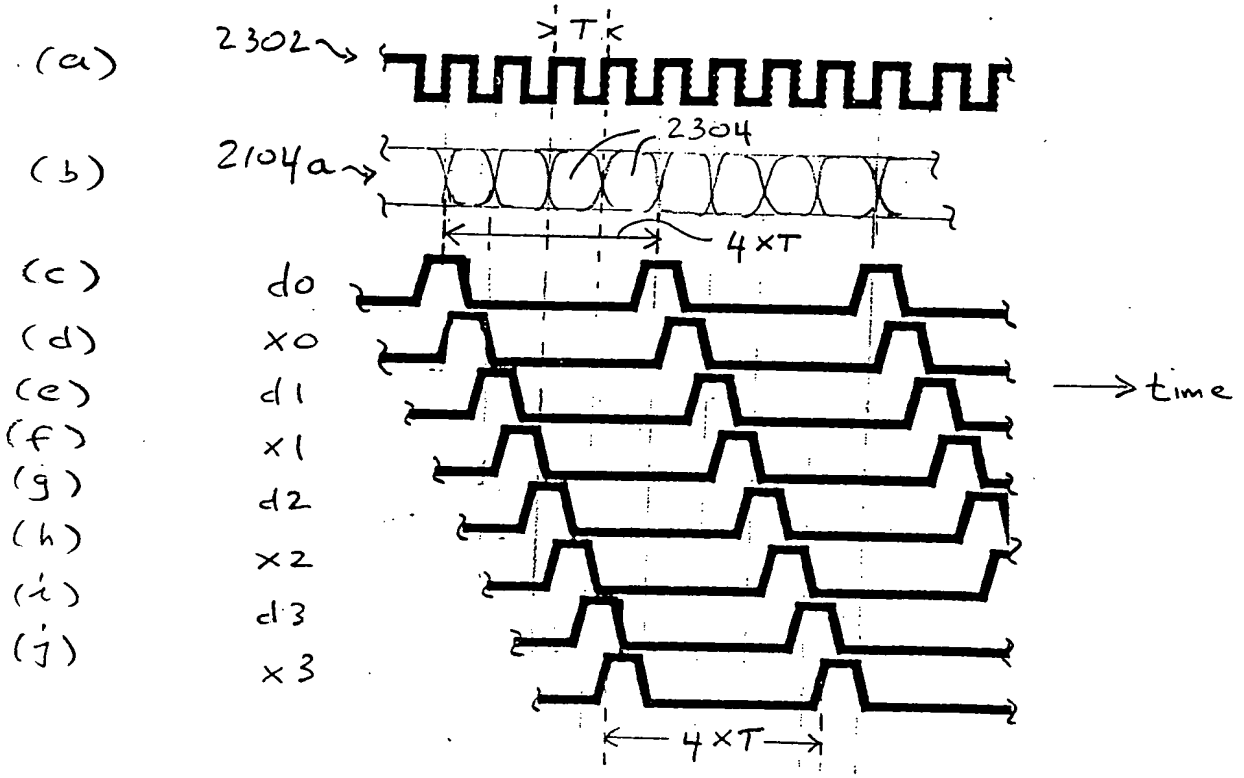

(a)
2302
T
(b)
2104a
2304
4×T
(c)
d0
(d)
x0
(e)
d1
(f)
x1
(g)
d2
(h)
x2
(i)
d3
(j)
x3
time
4×T

FIG. 23

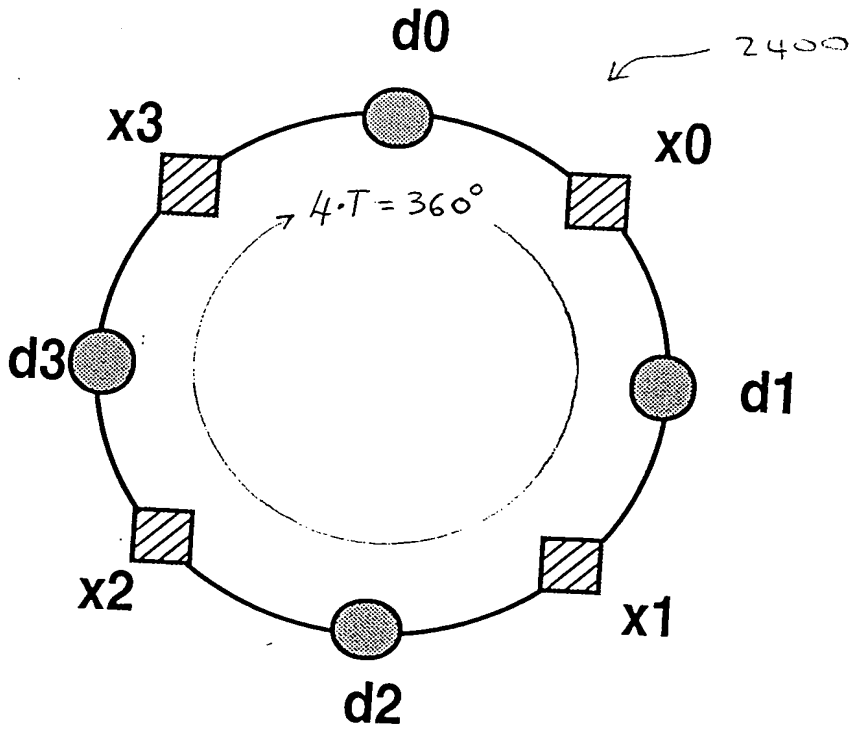

d0
2400
x3
x0
4·T = 360°
d3
d1
x2
x1
d2

FIG. 24

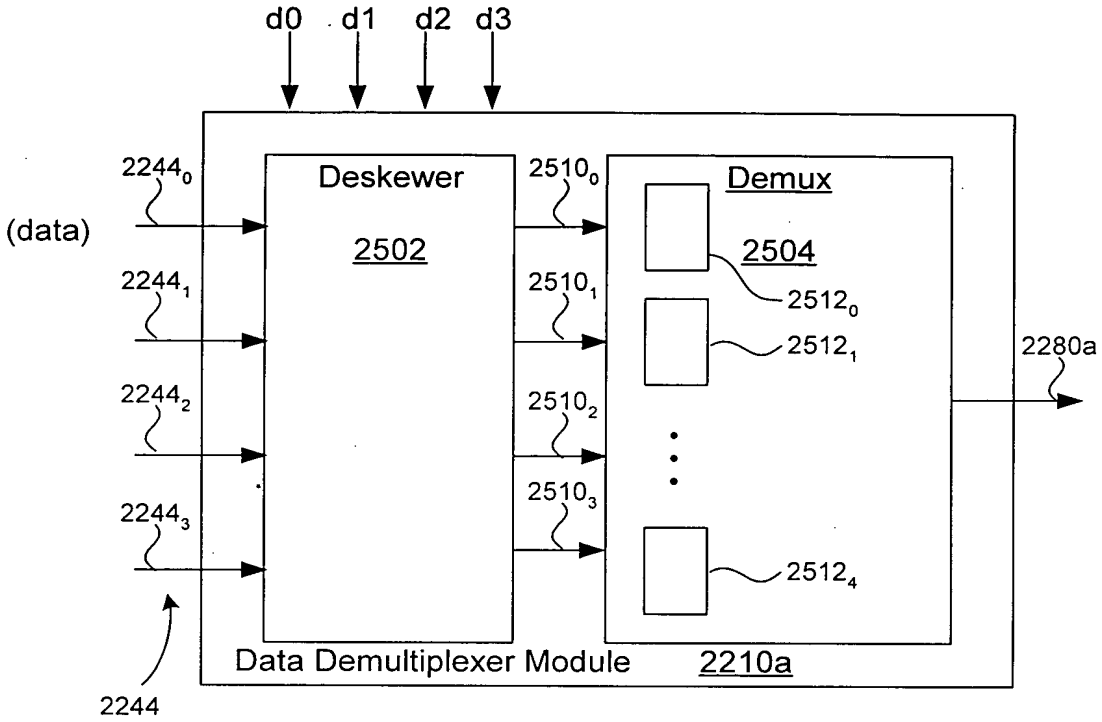

d0
d1
d2
d3
(data)
2244$_0$
2244$_1$
2244$_2$
2244$_3$
2244
Deskewer
2502
2510$_0$
2510$_1$
2510$_2$
2510$_3$
Demux
2504
2512$_0$
2512$_1$
2512$_4$
2280a
Data Demultiplexer Module
2210a

FIG. 25

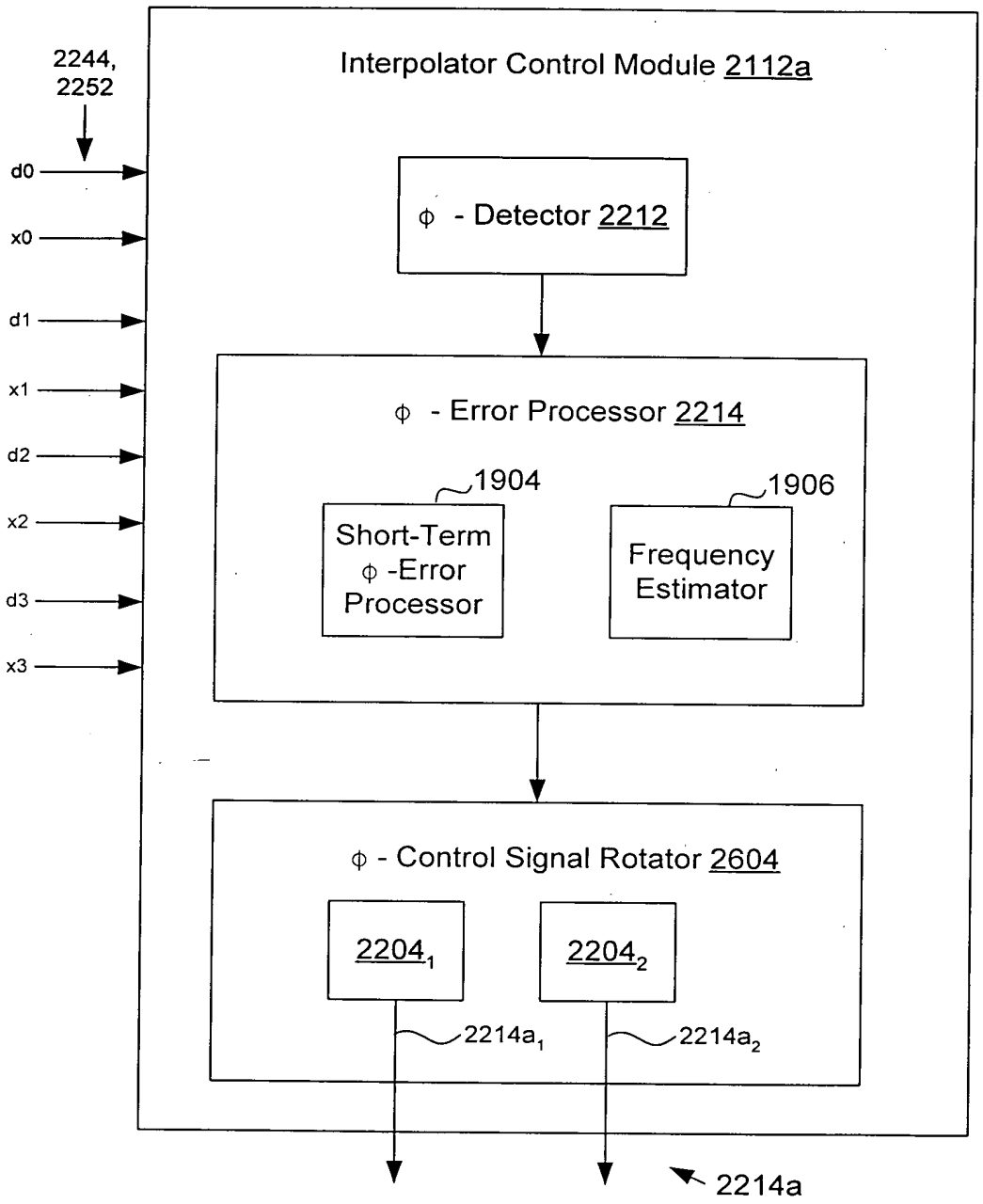

2244,
2252
Interpolator Control Module 2112a
d0
x0
d1
x1
d2
x2
d3
x3
ϕ - Detector 2212
ϕ - Error Processor 2214
1904
1906
Short-Term
ϕ -Error
Processor
Frequency
Estimator
ϕ - Control Signal Rotator 2604
2204$_1$
2204$_2$
2214a$_1$
2214a$_2$
2214a

FIG. 26

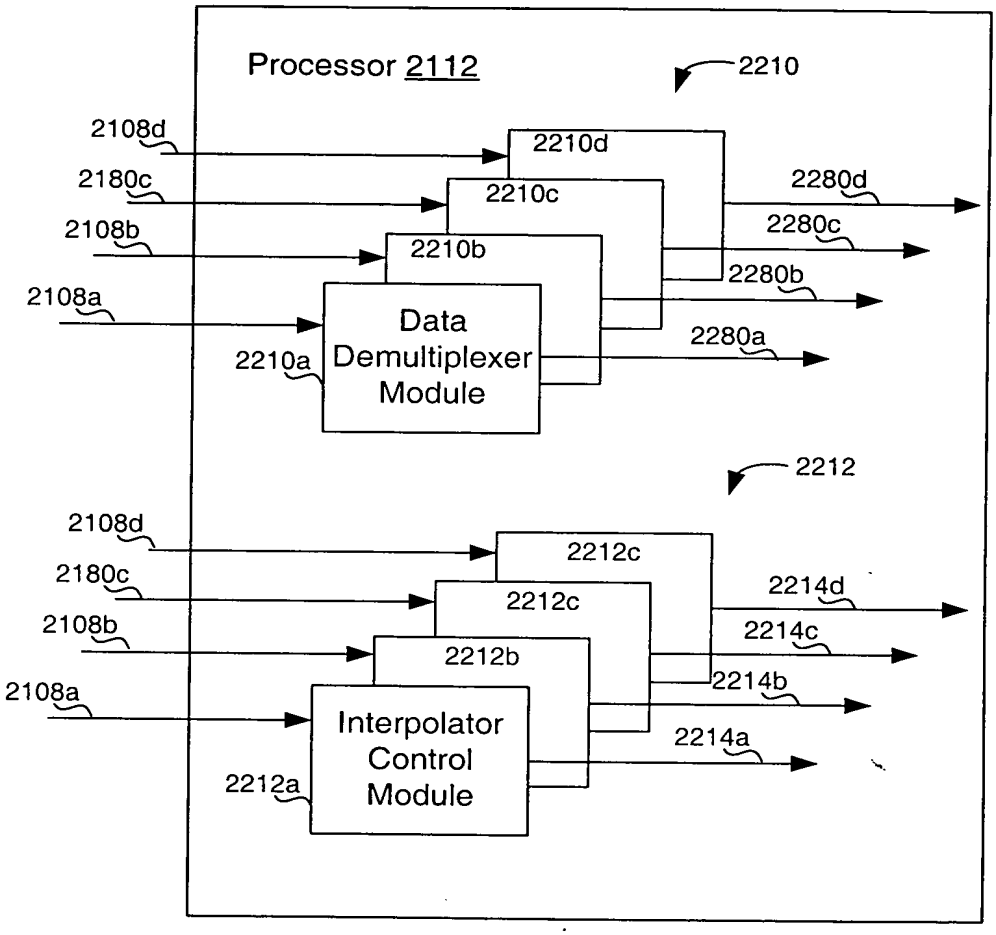

Processor 2112
2210
2108d
2210d
2180c
2210c
2280d
2108b
2210b
2280c
2280b
2108a
Data
Demultiplexer
Module
2210a
2280a
2212
2108d
2212c
2180c
2212c
2214d
2108b
2212b
2214c
2214b
2108a
Interpolator
Control
Module
2214a
2212a

FIG. 27

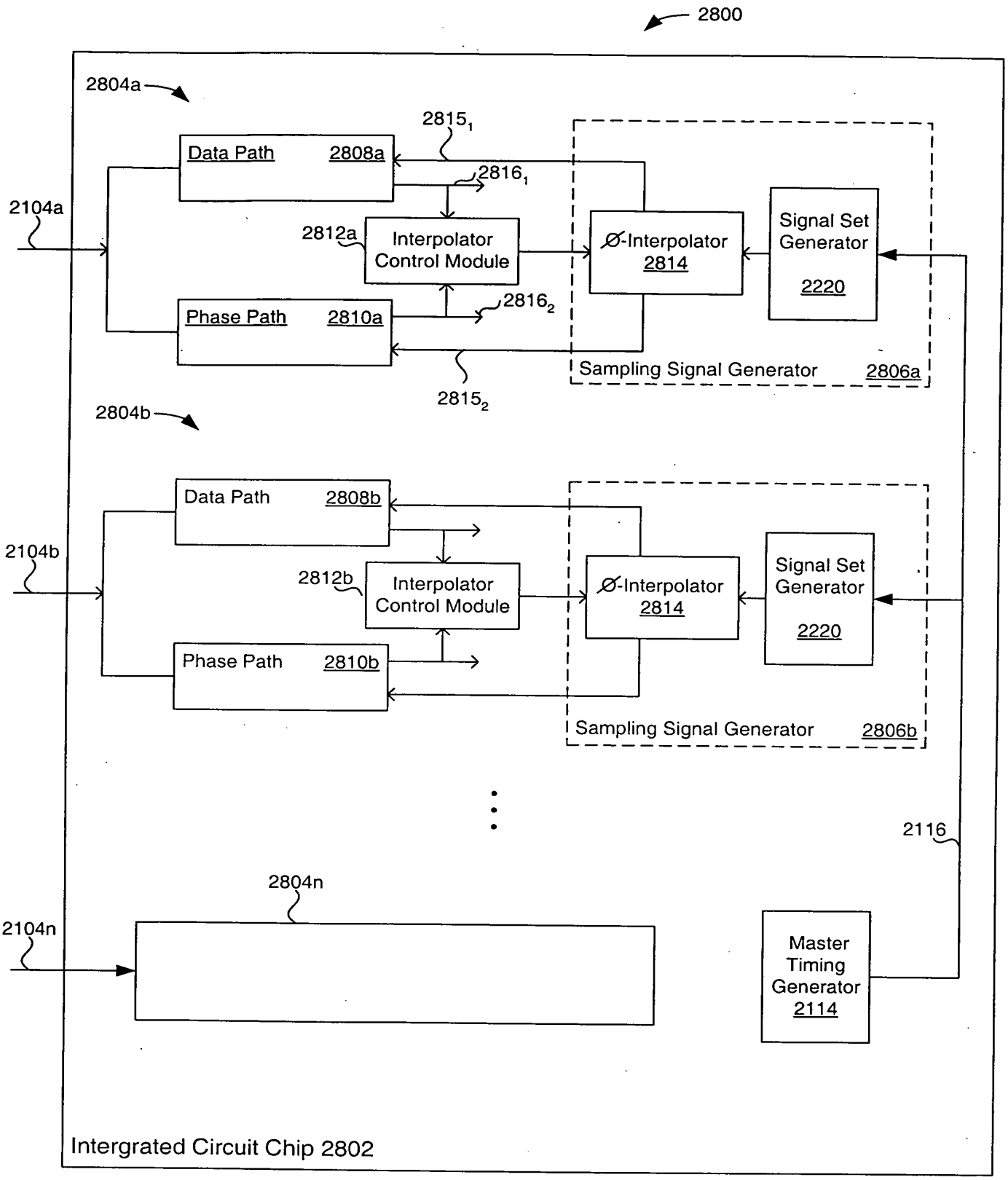

2800
2804a
2815$_1$
Data Path 2808a
2816$_1$
2104a
2812a
Interpolator Control Module
Ø-Interpolator 2814
Signal Set Generator 2220
Phase Path 2810a
2816$_2$
Sampling Signal Generator 2806a
2815$_2$
2804b
Data Path 2808b
2104b
2812b
Interpolator Control Module
Ø-Interpolator 2814
Signal Set Generator 2220
Phase Path 2810b
Sampling Signal Generator 2806b
2116
2804n
2104n
Master Timing Generator 2114
Intergrated Circuit Chip 2802

FIG. 28

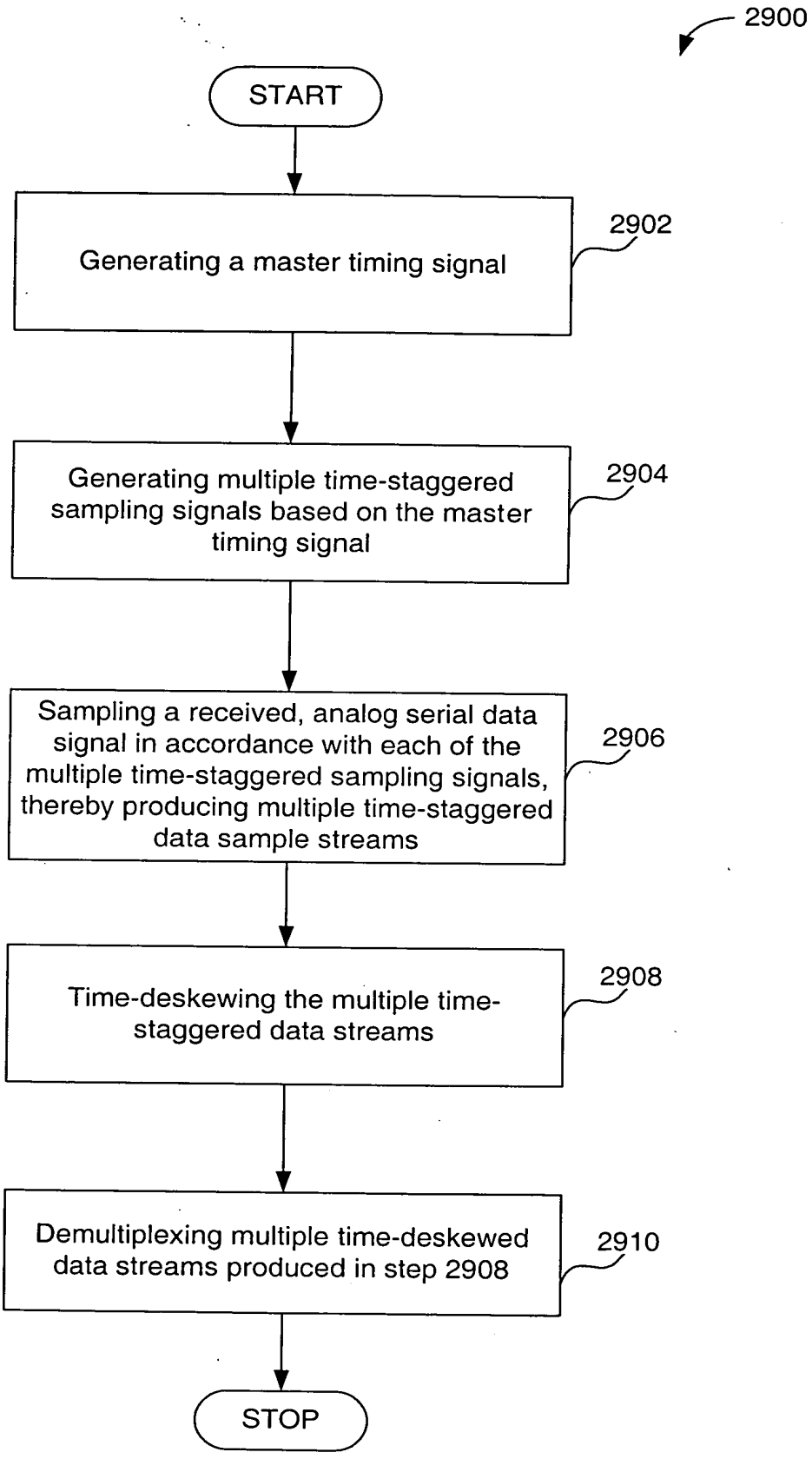


FIG. 29

0102-03.vsd/1

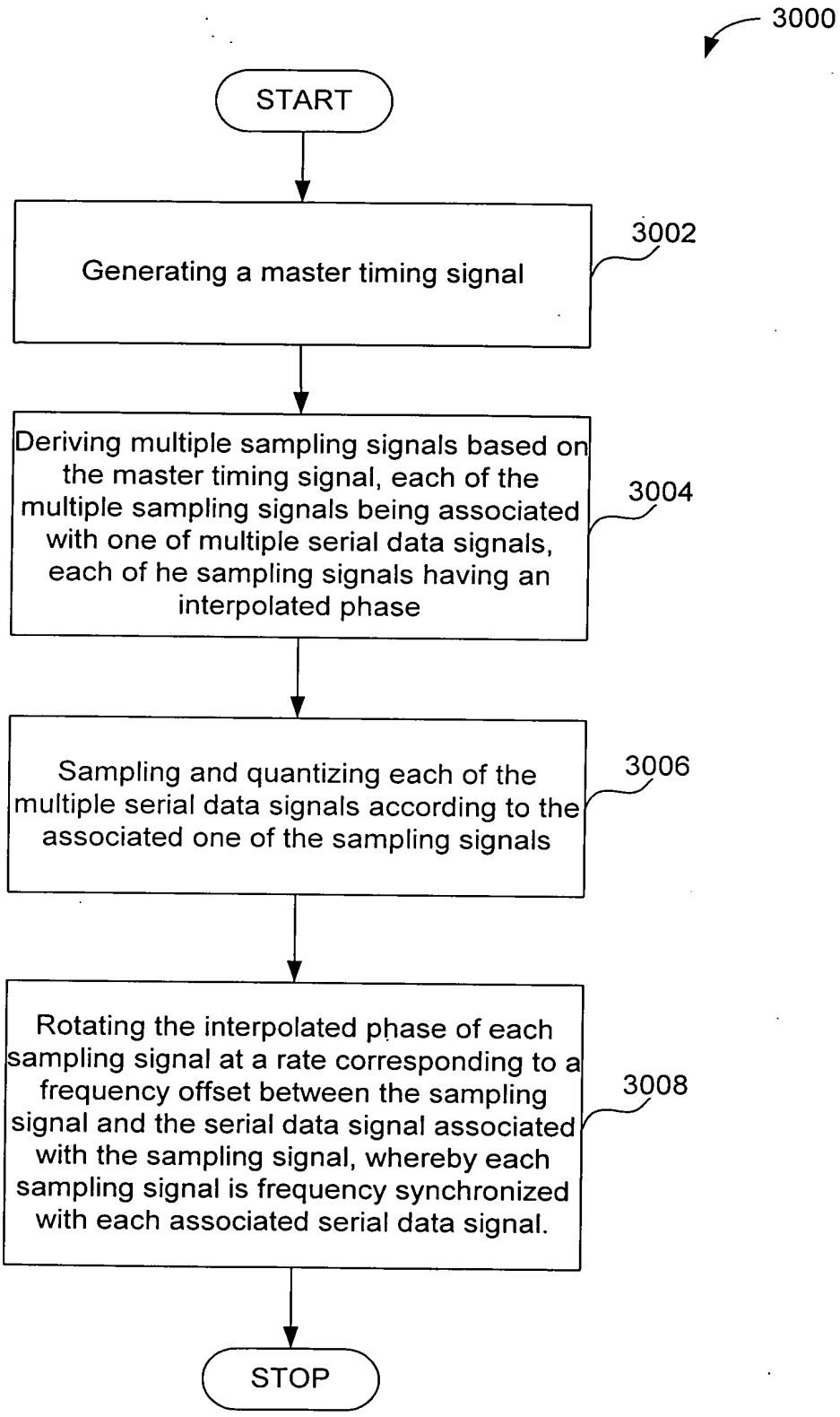


FIG. 30

0102-03.vsd/2

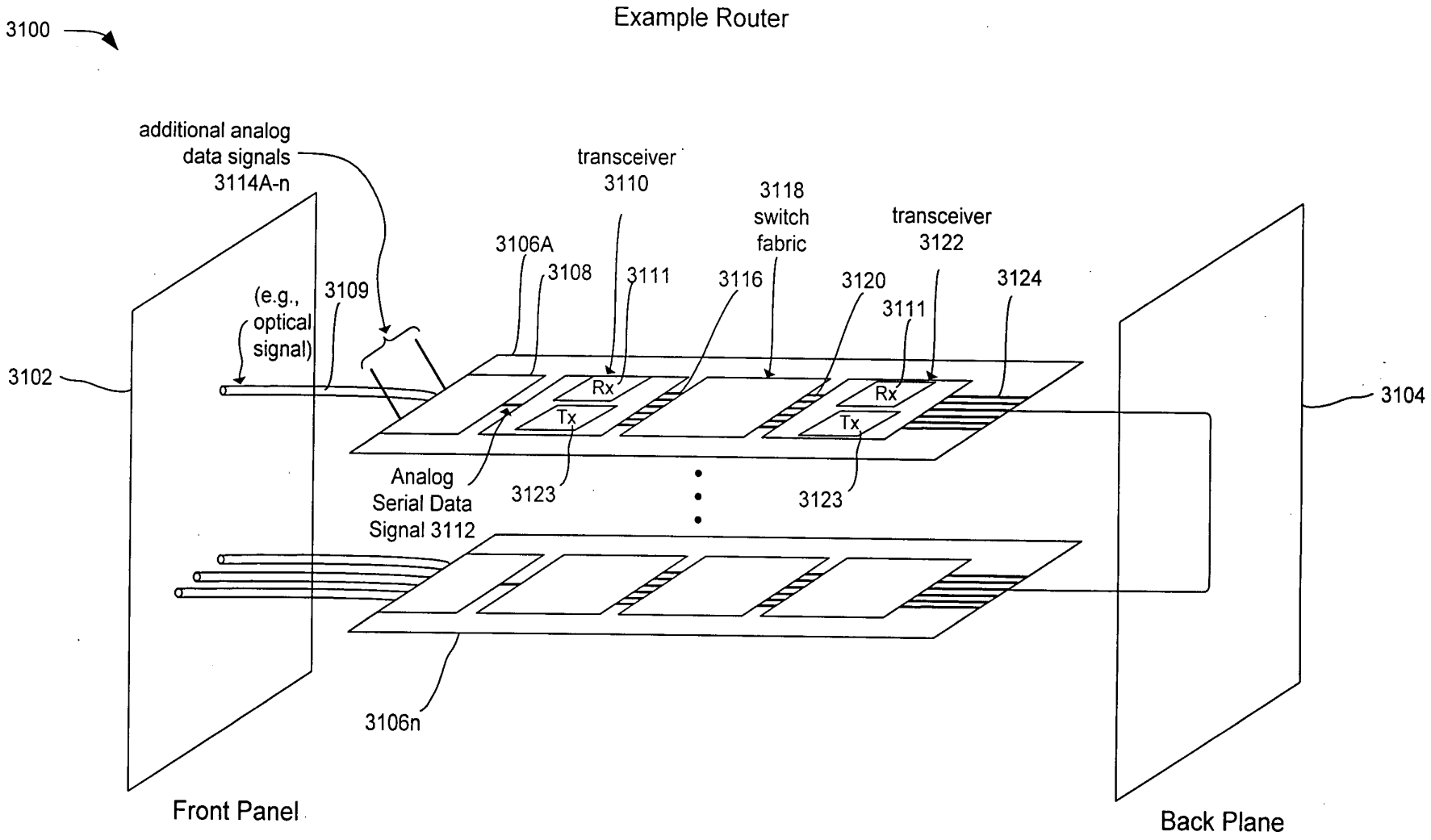


FIG. 31

0102-03.vsd/3

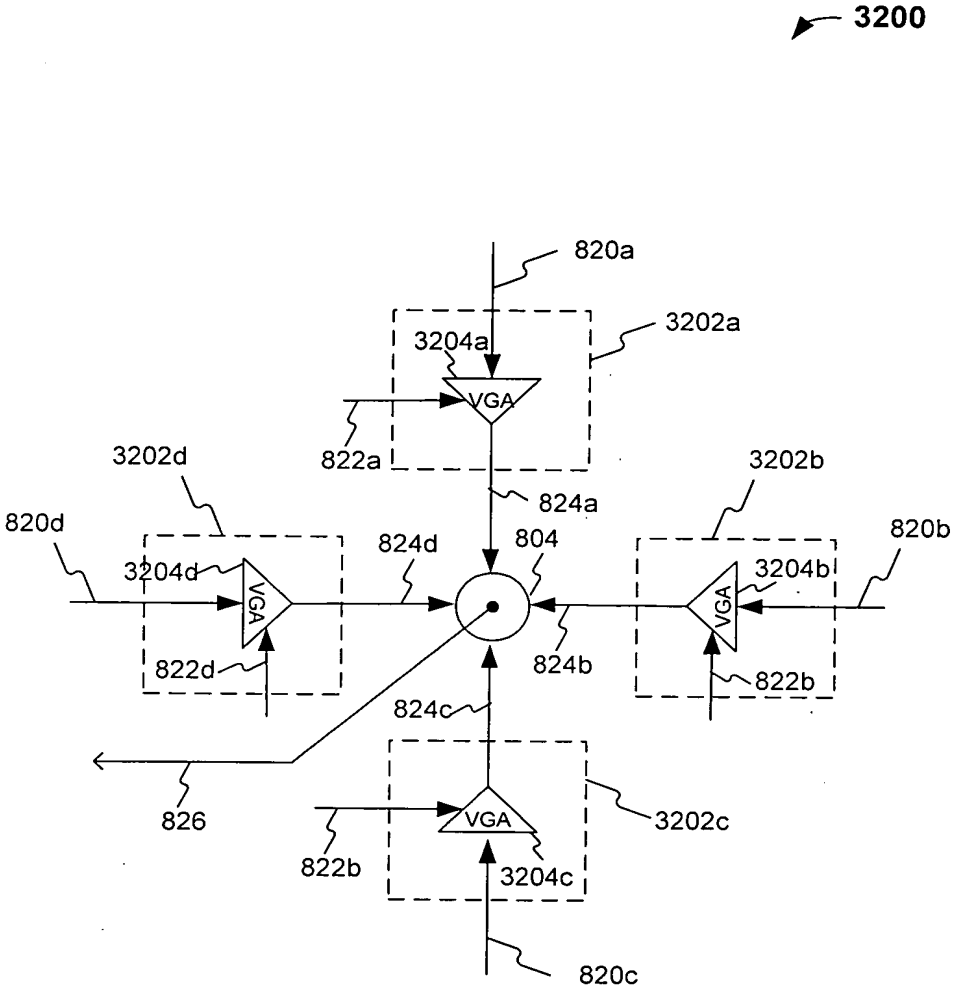

3200
820a
3202a
3204a
VGA
822a
3202d
3202b
824a
820d
820b
824d
804
3204d
3204b
VGA
VGA
822d
824b
822b
824c
826
3202c
VGA
822b
3204c
820c

FIG. 32

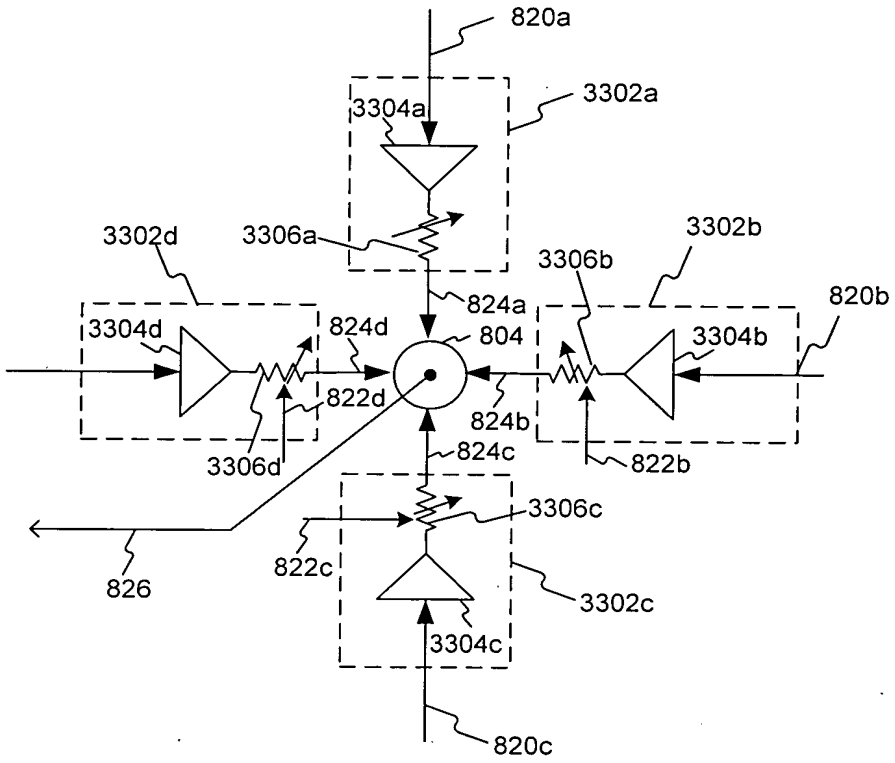

3300
820a
3302a
3304a
3306a
3302d
3306b
3302b
820b
824a
3304d
824d
804
3304b
822d
824b
824c
3306d
822b
3306c
822c
826
3302c
3304c
820c

FIG. 33

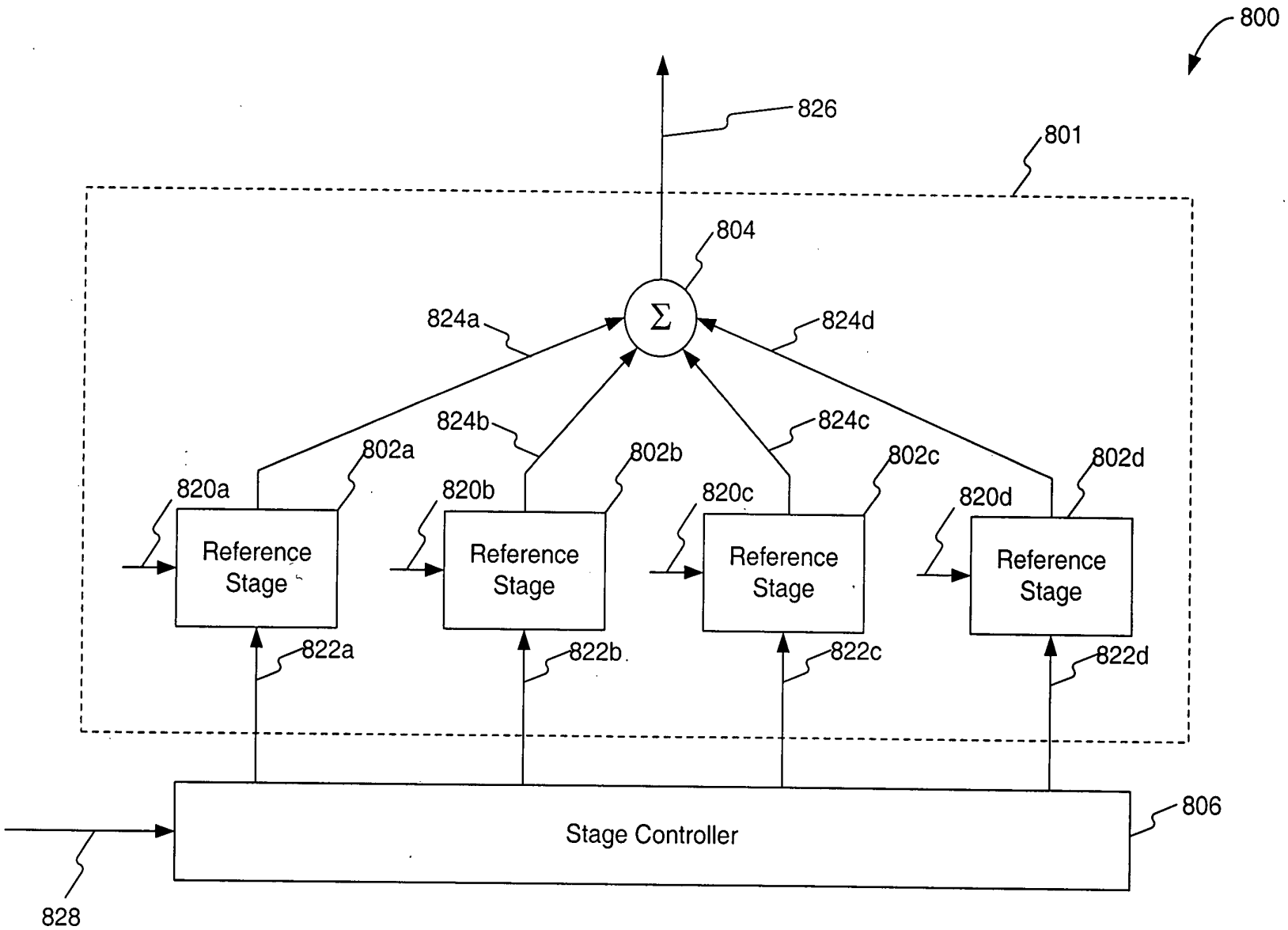

800
826
801
804
Σ
824a
824d
824b
824c
802a
802b
802c
802d
820a
820b
820c
820d
Reference Stage
Reference Stage
Reference Stage
Reference Stage
822a
822b
822c
822d
Stage Controller
806
828

FIG. 8

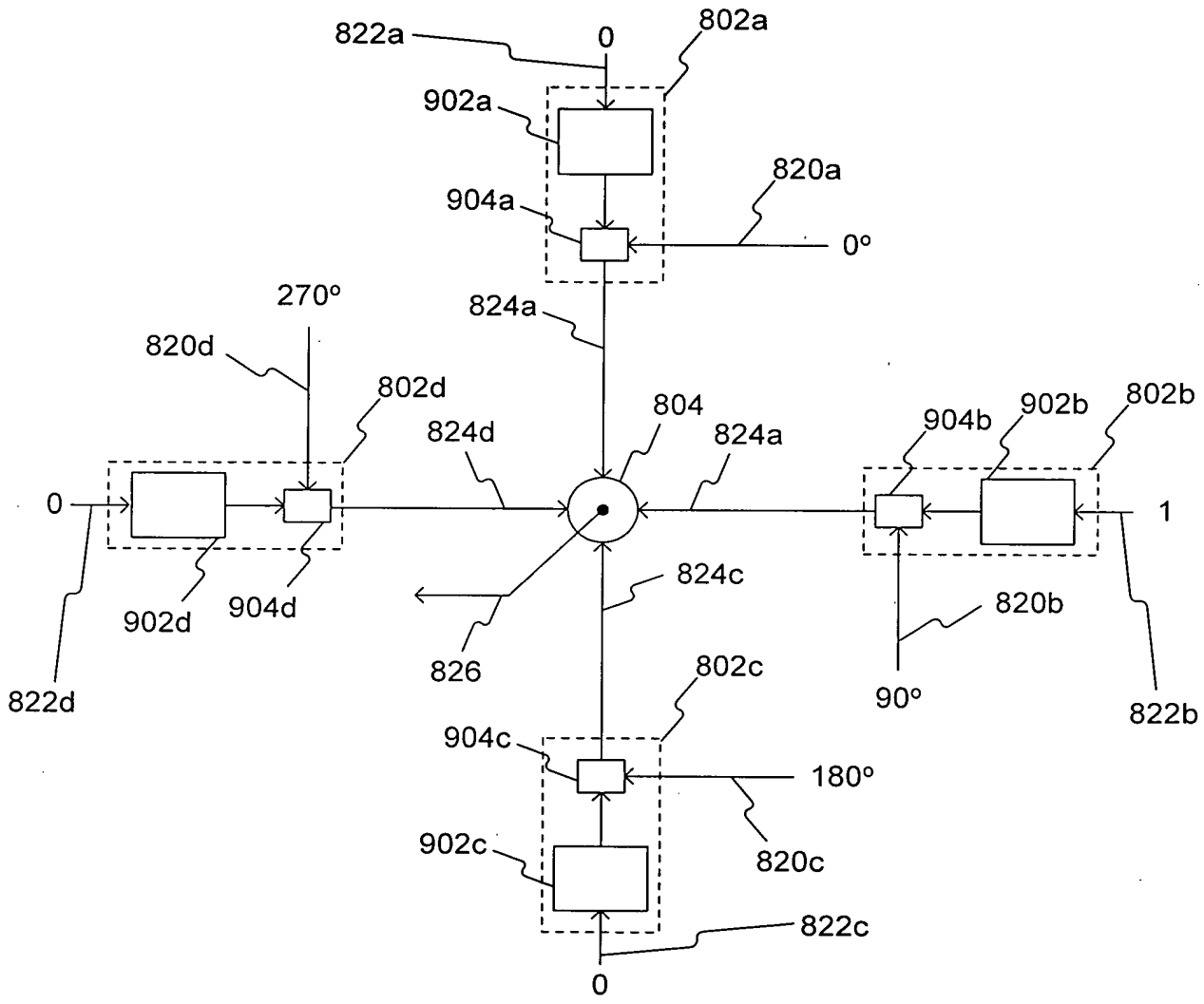

822a
0
802a
902a
820a
904a
0°
270°
824a
820d
802d
804
824d
824a
904b
902b
802b
0
1
902d
904d
824c
820b
826
802c
90°
822d
822b
904c
180°
902c
820c
822c
0

FIG. 9

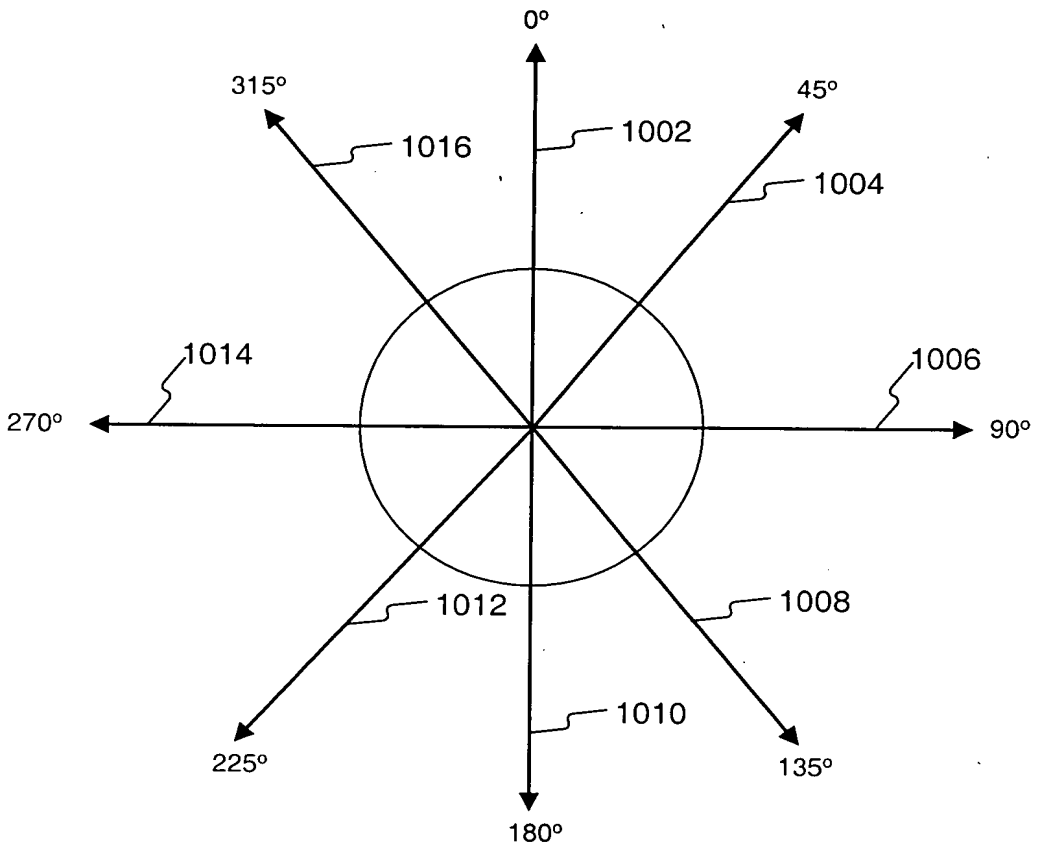

0°
315°
45°
1016
1002
1004
1014
1006
270°
90°
1012
1008
1010
225°
135°
180°

FIG. 10

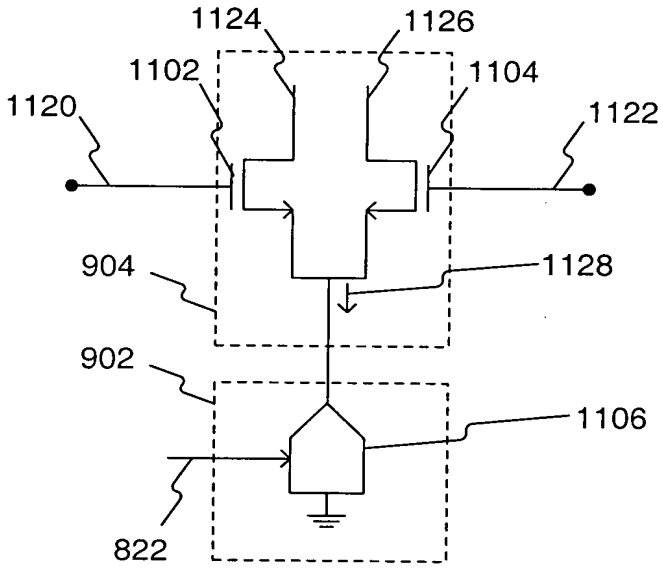


FIG. 11

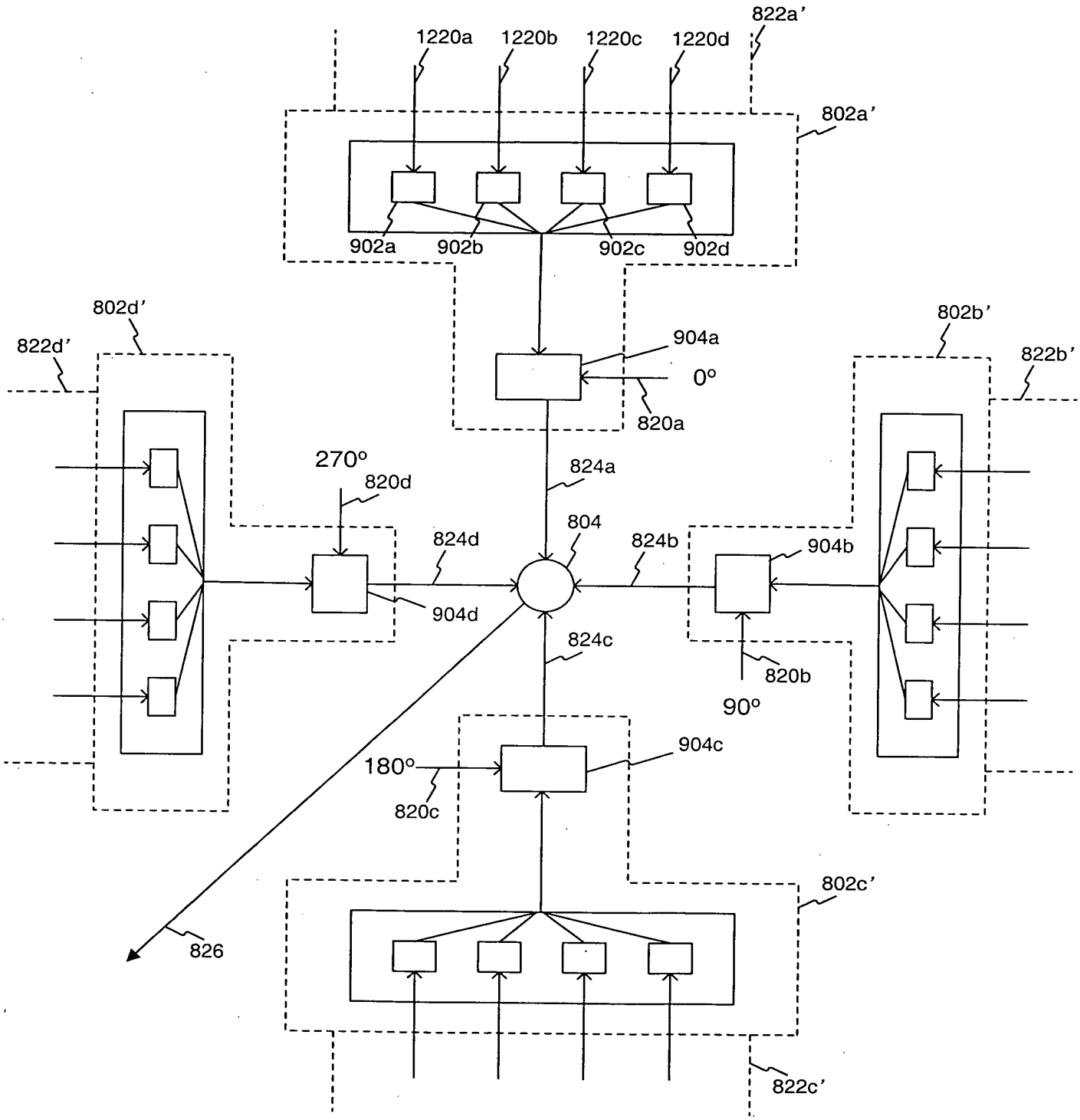


FIG. 12

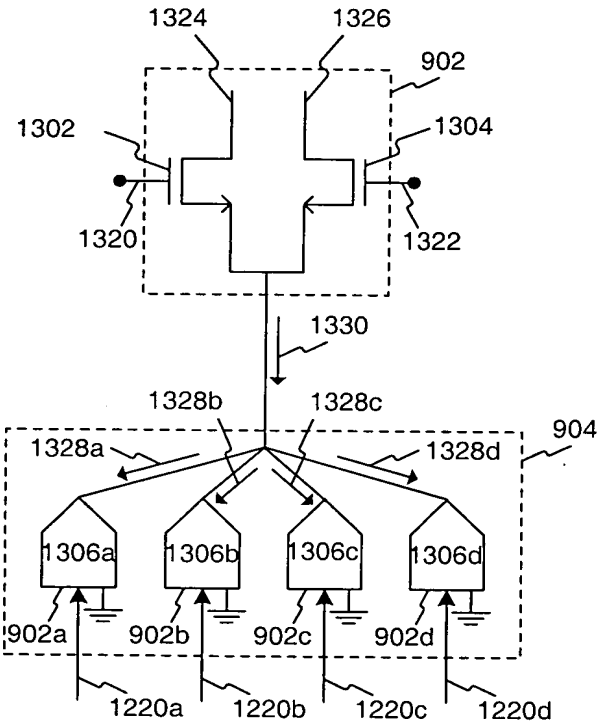

1324
1326
902
1302
1304
1320
1322
1330
1328b
1328c
904
1328a
1328d
1306a
1306b
1306c
1306d
902a
902b
902c
902d
1220a
1220b
1220c
1220d

FIG. 13

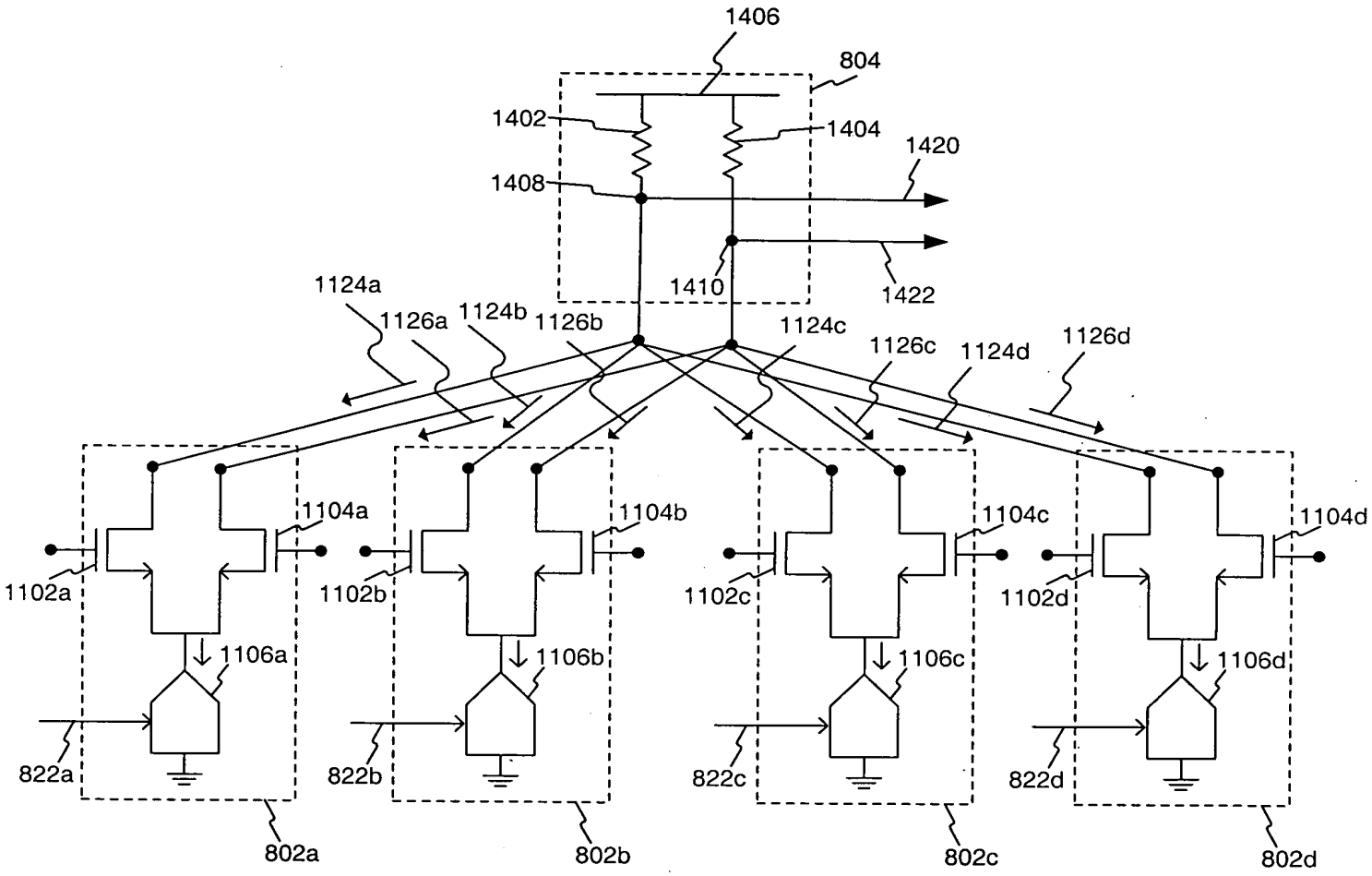

1406
804
1402
1404
1420
1408
1410
1422
1124a
1126a
1124b
1126b
1124c
1126c
1124d
1126d
1104a
1104b
1104c
1104d
1102a
1102b
1102c
1102d
1106a
1106b
1106c
1106d
822a
822b
822c
822d
802a
802b
802c
802d

FIG. 14A

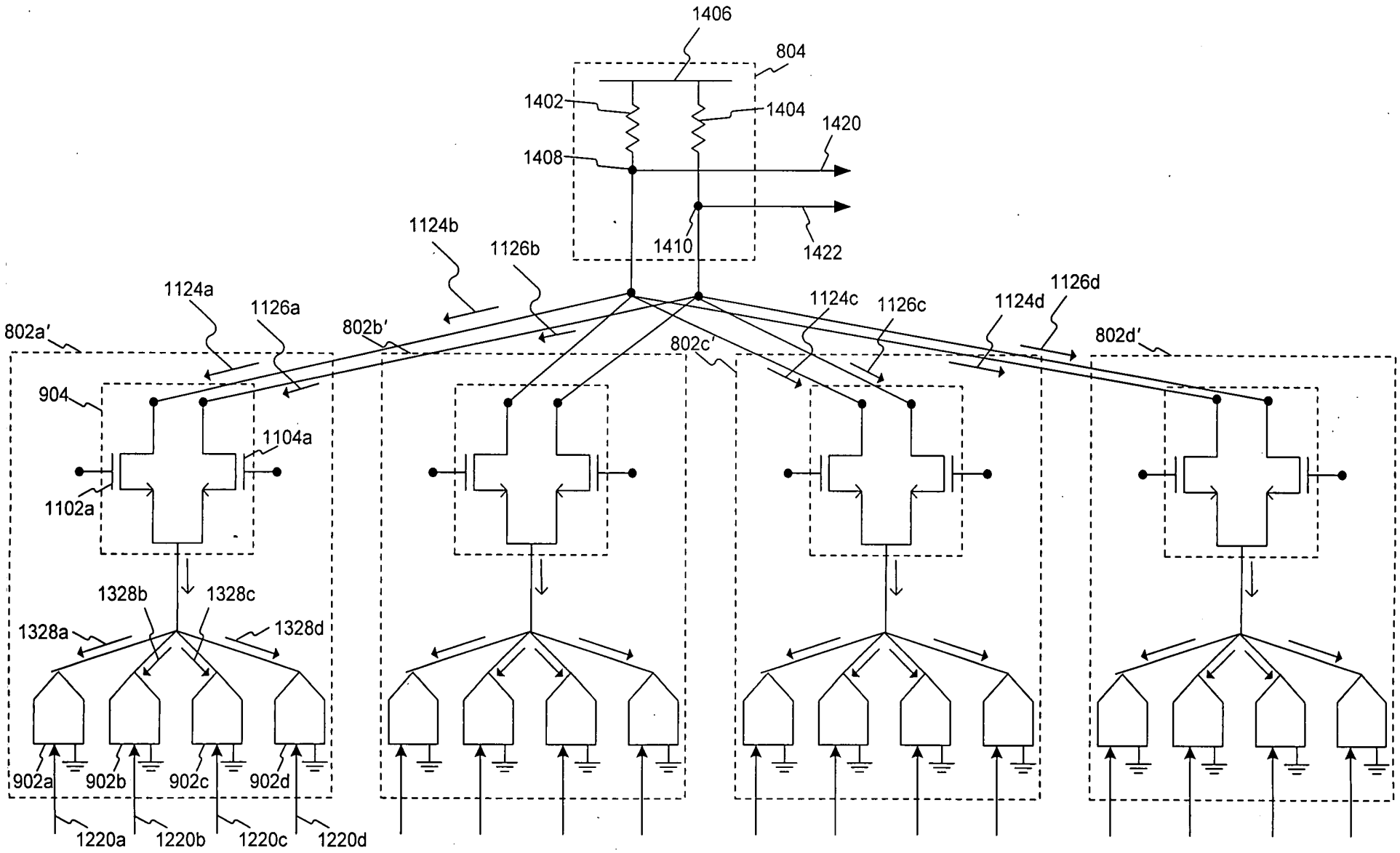

1406
804
1402
1404
1420
1408
1422
1410
1124b
1126b
1124a
1126a
802a'
802b'
802c'
1124c
1126c
1124d
1126d
802d'
904
1104a
1102a
1328b
1328c
1328a
1328d
902a
902b
902c
902d
1220a
1220b
1220c
1220d

FIG. 14B